PONE-D Electronics Interface Control Meeting Agenda (Flasher + MIST + Interposer + Mainboard + Ubase)

Project + Interfaces: PONE-D mainboard-interposer-Flashers-µBase, MIST

Date: -04-2026

Attendees:

Document Version: R0

Agenda Overview

- Interposer ↔ Flashers Interface
- Interposer/Mainboard ↔ MIST System Interface
- Interposer ↔ uBase (PMTs)
- Mainboard ↔ Interposer Signals
- Mainboard ↔ Interposer Physical Interface

Key Decisions Reviewed

- Flasher timing requirements and control architecture
- Digital vs analog interface strategy with MIST
- DAC threshold implementation location
- Communication protocol for uBase (UART vs I2C)
- Final signal and power mapping (Mainboard ↔ Interposer)
- Connector and cable selection (Mainboard ↔ Interposer)

1 Interposer ↔ Flashers Interface Details

Options:

1) A required change to interposer-Flasher interface is altering the use of custom rigid-flex cables, as detailed in various "lessons learned". Easiest and cheapest option is use of low profile ethernet cables that could immediately replace all signals + power required.
2) It has been discussed that the flash-start signal will not be used in analyses, so its timing is not critical, so flash start signal could be generated on interposer, potentially allowing simplification of switching/routing scheme to flashers.
3) THere will be less flashers in each optical module - how many will be included and where will they be located?
4) If observer channel desired to be used for TDC should reconfigure to an amplify and hold signal, since smaller pulse width and amplitude from earlier versions is not reliably picked up from interposer now. Alternatively, can remove all circuitry for this and not use for TDC out.
5) If pulse delay is not required to set pulse width (all flashers use RC circuit to determine pulse width), or if flashers on calibration only use longer pulse widths, and others use RC circuit-could alter delay chip to one with more modern interface, uses 3.3V. Can also remove dual differential signals to each flasher
6) Can look at using different clock buffer that uses 3.3V and 8 outputs, or different simpler switching scheme depending on result of previously listed options.
7) If none of the flashers will use voltages > 40V, can reduce the HV supply to 45V (reduces ripple output), can reduce current limiting resistor.

Discussion Notes:

Technical Considerations:

Risks / Concerns:

Final Decisions:

Action Items (Owner / Due Date):

2 Interposer + Mainboard ↔ MIST System Interface Details

Options:

1) We can use current system where comparator + threshold is performed on interposer. Then the connectors between interposer and MIST needs to be defined (can see associated previous documents for options). Assume using same connector
2) Utilize separate connector for MIST on mainboard (whether or not signals come from interposer). This allows less connections/cables as one interposer-mainboard connection does not require these connections.
3) If there is a separate connector for MIST then output could go directly from MIST to mainboard. This required conversion to digital via threshold/comparator circuit to be on MIST module. If this is done then threshold voltage either transferred to MIST module from interposer, or DACs on MIST controlled by I2C are implemented.
4) Bypass interposer completely and send I2C + power with same connector carrying signals. Since bias voltage is generated on interposer not sure how to resolve this cleanly. Probably don't want to generate HV on mainboard, since varies and also goes to flashers and calibration board SiPM and don't want to replicate same HV generation on MIST.

Discussion Notes:

Technical Considerations:

Risks / Concerns:

Final Decisions:

Action Items (Owner / Due Date):

3 Interposer ↔ uBase Interface Details

Options:

1) Original v1 with just altered latch connector and resistors
2) V2 with I2C interface
3) V2 with UART interface and latched connector (slightly changed)

Discussion Notes:

Technical Considerations:

Risks / Concerns:

Final Decisions:

Action Items (Owner / Due Date):

4 Mainboard ↔ Interposer Interface Details

Options:

1) In redesign of interposer and the proposed use of I2C for ubase, there is more motivation to change interposer control interface to I2C instead of SPI. Most control chips on interposer can alternatively use I2C, or there are versions that use I2C. This will reduce the number for lines required (also switching GPIOs for SPI not needed) and simplify interface.
2) The use of Flasher start pulse may be unnecessary and could instead be generated on interposer with I2C interface + GPIO expander + analog circuitry to reduce rise rime and control duration.

Original-Utilize PONE-1 interface	Option 1-alter to I2C, remove FLASH_IN,	Option 2-Include additional optional connections, MIST separate connection	Option 3-
1-5V, 2-5V 3-GND, MIST4 5 -MIST3, MIST 2 7-GND, MIST 1 9-UART Rx, 10-UART Rx 11-GND, 12-GND 13-GPIO A1, 14-GPIO A2 15-GND, 16-GND 17-CS, 18-GPIO A0 19-MOSI, 20-GND 21-MISO, 22-GPIO RST 23-CLK, 24-GND 25-GND, 26-FLSH_TDC 27-GND, 28-GND 29-Piezo_N, 30-Piezo_P 31-GND, 32-GND 33-GND, 34-FLASH_IN 35-GND, 36-GND 37-3.3V, 38-3.3V 39-1.8V, 40-1.8V	1-SDA, 2-SCL 3-GPIO RST, 4-3.3V 5-Piezo P, 6-Piezo N 7-TDC P, 8 –TDC N (GNDs depends on cable) 11-MIST 1, 12-MIST 2 13-MIST 3, 14-MIST 4	Pinout D-shaped, e.g. micro-D (21 pins): P * g T g R I G 3 3 G P * g T g I G 1 1 G P P g T g R I G 3 3 G * * g T g g I G 1 1 G Key: G: Ground attached on both ends g: Ground attached on mainboard only (drain) P: Piezo hydrophone +/- *: Second hydrophone +/- or ground (g) -- could also be dropped T: Flasher_TDC +/- (from interposer, LVDS?) R: RESETB to interposer (3.3V) I: I2C SCL/SDA (3.3V) 3: 3.3V 1: 1.8V	

Discussion Notes:

Technical Considerations:

Risks / Concerns:

Final Decisions:

Action Items (Owner / Due Date):

5 Connector + Cable Choice (Mainboard ↔ Interposer)

Requirements:

1) Fit through MIST module opening, and make plate hole + turn
2) High speed capability
3) Shielding
4) Power delivery
5) Mechanical latch/screw-down
6) Polarized
7) Integration Complexity
8) Cost

Table 1: Decision matrix for connector/cable choice

	Requirements							
Connector/System	1	2	3	4	5	6	7	8
	MIST opening	High speed	Shielding	Power	Latch	Polarized	Complexity	Cost
Molex 87833-4020 (40-pin) and ribbon cable	↓	↓	↓	↑	↓	↓	↔	↑
Molex 87833-4020 (40 pin) and custom assembly	↔	↓	↓	↑	↓	↓	↔	↓
Samtec HLCD + LSHM (microcoax)	↑	↑	↑	↑	↔	↑	↔	↓
Micro-D Connector + cable (assume specialized/custom cable for high speed/shielding)	↔	↑	↑	↑	↑	↑	↑	↓
Multi-Connector System (MicroLock + locking SATA + SFSD)	↑	↑	↑	↑	↑	↑	↔	↑

5.1 Notes on Connectors:

Molex 87833-4020:

Pro: single connector, power handling is suitable, through hole board connection **Con:** No matching 40-pin wire mating receptacle; ribbon unsuitable; requires custom cable (partially twisted pairs); no shielding; friction fit only (requires second mechanical latch), no polarizing key. **Cost:** ribbon cable (~$20 CAD), custom cable (~$150 CAD)

Samtec LSHM:

Pro: multiple hermaphrodite connector options, power handling is suitable, through hole board side connector, shielded, impedance controlled, commercially available cable

assemblies, can obtain screw down option for cable, **Con:** SM connections for signal lines, low mating cycles, requires custom mechanical fixture for screw down **Cost:** commercial cable (~$80 CAD)

Micro-D Connector + cable

Pro: screw in option, high power, rigid **Con:** large profile, different options (right angle etc.) more expensive, direct to manufacture purchase likely required (time to negotiate), not impedance matched (unless specialized), not for high-speed (unless specialized) **Cost:** non-specialized commercial cable (~$100 CAD)

Multi-Connector System (Micro-Lock/Fit + locking SATA + SFSD)

Pro: polarized connections, through hole connectors, latching connector, optimized for signal/power/speed, shielded, impedance controlled, commercially available cable assemblies **Con:** need to zip-tie cables together **Cost:** commercial cables (~$15 CAD)

Other Options

- Mixed signal systems from Samtec, Harwin or other (optimized for all requirements, but expensive and long lead time, possible missing in future)

Discussion Notes:

Technical Considerations:

Risks / Concerns:

Final Decisions:

Action Items (Owner / Due Date):