UG0750
User Guide
PolarFire FPGA I/O Editor

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Revision History

The following table shows important changes made in this document for each revision.

Revision	Changes
Revision 1 (January 2017)	Initial release
Revision 2 (May 2017)	Updated Memory View and IOD view and updated graphics
Revision 3 (October 2017)	Revision 3 includes the following changes: • Added Chapter 9, Floorplanner View • Added Chapter 10, Other Windows • Updated I/O attribute information in Chapter 3, Pin View • Updated figures to reflect new tab order and naming • Added information about Signal Integrity View in Chapter 7, XCVR View
Revision 4 (March 2018)	Revision 4 includes the following changes: • Updated I/O information in Chapter 2, Port View, and Chapter 3, Pin View • Minor edits for clarification in Chapter 4, Package View, Chapter 7, XCVR View, Chapter 8, IOD View, Chapter 9, Floorplanner View

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1 PolarFire I/O Editor

The PolarFire I/O Editor displays all assigned and unassigned I/O macros and their attributes in a spreadsheet-like format. Use the I/O Editor to view, sort, filter, select and set I/O attributes of the PolarFire device.

The I/O attributes can be viewed by port name or by package pin. Click the Ports View tab to view I/O attributes by port name. Click the Pin View tab to view I/O attributes by Pin name.

The PolarFire I/O Editor provides the following views for I/O assignment and planning:

- Port View - I/O spreadsheet sorted by port name
- Pin View - I/O spreadsheet sorted by pin number
- Memory View - I/O view specific to the memory interface
- IOD View - I/O view specific to the IOD Lane Controller interface
- XCVR View - I/O view specific to the transceiver interface
- Package View - Package Pin graphical view of the PolarFire device
- Floorplanner View - Detailed cell level device view of the entire chip

1.1 Invoking the PolarFire I/O Editor

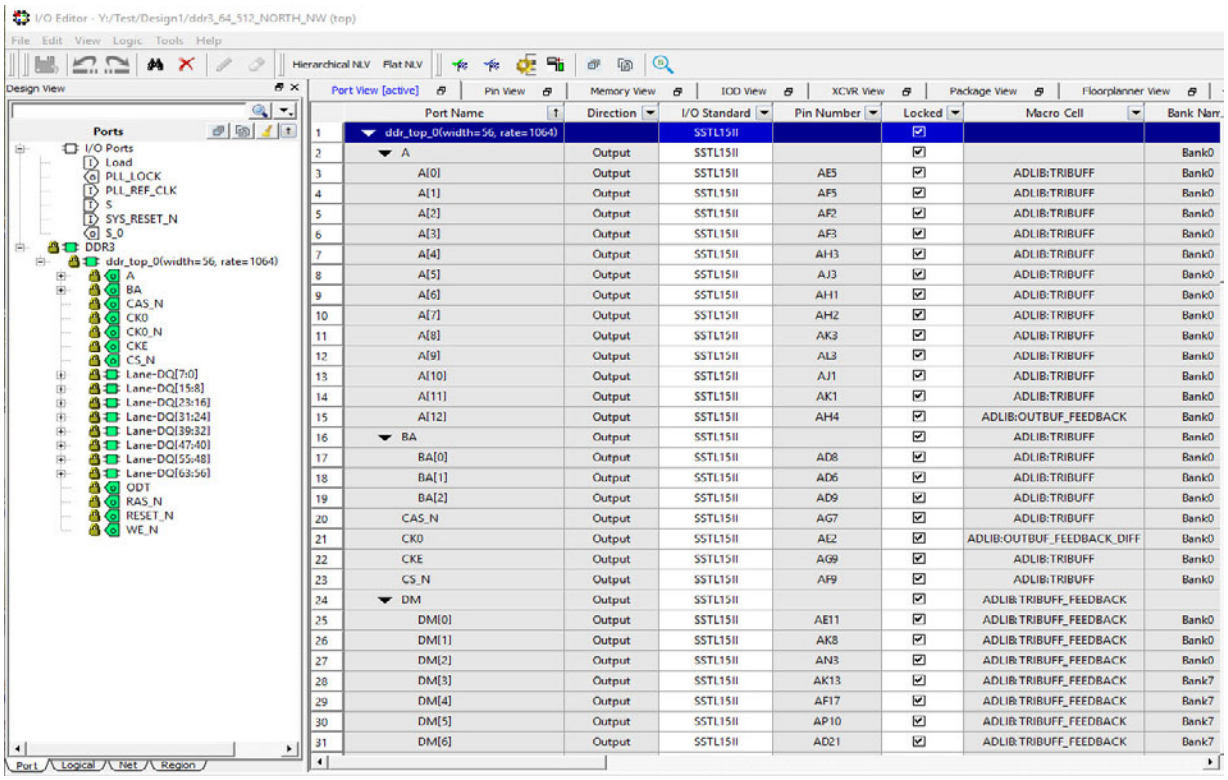
The design must be in the post-synthesis state before the I/O Editor can be invoked. A warning message appears if the I/O Editor is invoked in the pre-synthesis state.

To invoke the PolarFire I/O Editor:

1. Complete the Synthesis step.
2. Invoke the Constraint Manager from the Design Flow window (**Design Flow > Manage Constraints > Open Manage Constraints View)**.
3. In the Constraints Manager, select the I/O Attributes tab and then select Edit > Edit with I/O Editor (**I/O Attributes > Edit > Edit with I/O Editor**).

The I/O Editor opens with view tabs across the top of the graphical interface.

Figure 1 • **PolarFire I/O Editor**



2 Port View

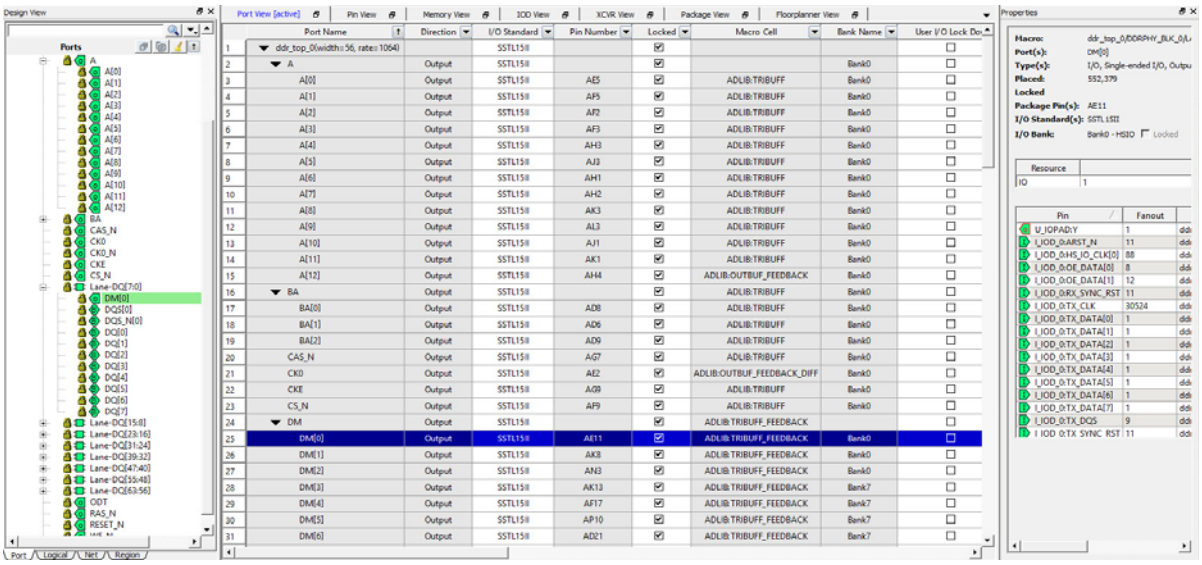
The Port view displays the PolarFire I/O attributes in a spreadsheet-like format. Each row corresponds to an I/O port in the design, sorted by the port name.The column headings specify the names of the I/O attributes in your design. The first four column headings are standard for all families so they will not change. For some I/O attributes, you will choose from a drop-down menu; for others, you might enter a value and for others, the field is read-only and not editable.

The display in the columns can be sorted alphabetically, numerically or filtered.

In the PolarFire I/O Editor, the ports are displayed in a spreadsheet-like format and also in the Design Tree View window under the Port tab. A port selected in the Port tab in the Design Tree view is also selected in the Port View spreadsheet and vice versa. Figure 2 · Port View shows the DM[0] selected in the spreadsheet and the Design Tree port view.

The Port View also displays the memory width and data rate of the DDR instance in the design (if it exists in the design) in the top left row under the Port Name column as shown in Figure 2.

Figure 2 • **Port View**



2.1 Port Name

This is the port list of the design. The ports of the design are displayed in a structured manner according to group name/functions. Ports can be expanded or collapsed. The port list can be sorted, or filtered, in a way similar to the Windows spreadsheet operations. Take for example, entering RESET in the match field in the filter returns a list of port names with the RESET in the port name.

2.2 Direction

Non-editable field that denotes Input, Output, or Inout.

2.3 I/O Standard

This field specifies the I/O standard the PolarFire device supports. Different I/O types have different I/O standards. The pull-down list displays the valid I/O standards for that particular type of I/Os. The list of valid I/O standards is limited to what the I/O bank (to which the I/O belongs) can support.

2.4 Pin Number

This is the package pin number specific to the die and package of the PolarFire device.

2.5 Macro Cell

This is a Read-only field that identifies the name of the Macro cell associated with the Port.

2.6 Bank Name

This is a read-only field to identify the I/O bank the I/O pin is associated with. Depending on the device size, PolarFire devices may have, six, or eight I/O Banks (Bank 0 through Bank 7) user I/O banks, Each pin is associated with an I/O bank. The I/O banks on the north side of the device support only HSIO. Each I/O bank has dedicated I/O supplies and grounds. Each I/O within a given bank shares the same V_{DDI} power supply, and the same V_{REF} reference voltage. Only compatible I/O standards can be assigned to a given I/O bank.

2.7 User I/O Lock Down

If checked, the current pin assignment cannot be changed during layout.

2.8 I/O State in Flash Freeze Mode

By default, all I/Os become tristated when the device goes into Flash*Freeze mode. You can override this default behavior by setting one of the following two values:

- LAST_VALUE - When set to this value, it preserves the previous state of the I/O. This means the I/O remains in the same state in which it was functioning before the device went into Flash*Freeze mode.
- LAST VALUE_WP - When set to this value, it preserves the last value with weak pull-up.

2.9 Clamp Diode

PolarFire devices have internal PCI clamp diodes for both HSIO and GPIO. PCI clamp diodes help reduce the voltage level at the input, and are mainly used when the voltage overshoot exceeds the maximum allowable limit. If signaling levels of the receiver are greater than the V_{DDIx} of the bank, the clamp diode must be off to support hot-socketing insertion.

For GPIO, use this field to program the clamp diode to be ON or OFF.

For HSIO, the internal clamp diode is always ON by default.

Table 1 • **Programmable Clamp Diode**

I/O Standard	Supported I/O Type	Clamp Diode Control
LVTTL	GPIO	OFF/ON
LVCMOS33	GPIO	OFF/ON
LVCMOS25	GPIO	OFF/ON
LVCMOS18	GPIO	OFF/ON
LVCMOS15	GPIO	OFF/ON
LVCMOS12	GPIO	OFF/ON
SSTL25	GPIO	OFF/ON

Table 1 • **Programmable Clamp Diode *(continued)***

I/O Standard	Supported I/O Type	Clamp Diode Control
SSTL18	GPIO	OFF/ON
SSTL15	GPIO	OFF/ON
HSTL15	GPIO	OFF/ON

2.10 Resistor Pull

Use this field to allow inclusion of a weak resistor for either pull-up or pull-down of the input buffer. The available options are None, Up (pull-up), Down (pull-down), or Hold. The default value is None, except when an I/O exists in the netlist as a port, is not connected to the core, and is configured as an output buffer. In that case, the default setting is for a weak pull-down.

Note: Not all I/O standards have a selectable resistor pull option.

2.11 Schmitt Trigger

PolarFire GPIO and HSIO can be configured as a Schmitt Trigger input. When configured as ON, it exhibits a hysteresis that helps to filter out the noise at the receiver and prevents double-glitching caused by noisy input edges. Default configuration is OFF (Schmitt Trigger disabled).

2.12 Vcm Input Range

Values for all I/O standards are MID, LOW. The default is MID.

2.13 On-Die Termination (ODT)

ODT is an option used to terminate input signals. Terminating input signals helps to maintain signal quality, save board space, and reduces external component costs. In PolarFire FPGAs, ODT is available in receive mode and also in bidirectional mode when the I/O acts as an input. If ODT is not used or not available, the PolarFire I/O standards may require external termination for better signal integrity.

ODT can be a pull-up, pull-down, differential, or Thévenin termination with both static and dynamic control available, and is set using either the Libero SoC software I/O attribute editor or by using a PDC command.

In addition, ODT can be controlled dynamically for individual I/Os as well as for all I/Os in a lane simultaneously on a per-lane basis.

Table 2 • **ODT Support in GPIO and HSIO**

I/O Standards	I/O Types (Input Only)	ODT Control	ODT Type	ODT Value (ohm)
LVDS33/LVDS25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
RSDS33/RSDS25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
MINILVDS33/ MINILVDS25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
SUBLVDS33/ SUBLVDS25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
LVPECL33/ LVPECL25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100

Table 2 • **ODT Support in GPIO and HSIO *(continued)***

I/O Standards	I/O Types (Input Only)	ODT Control	ODT Type	ODT Value (ohm)
SSTL18I/SSTL18II	GPIO, HSIO	Off/Static/Dynamic	Off/Thévenin	Off, 50, 75, 150
SSTL15I, SST15II	GPIO, HSIO	Off/Static/Dynamic	Off/Thévenin	Off, 20, 30, 40, 60, 120
RSDS33/RSDS25/	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
HSTL15I/HSTL15II	GPIO	Off/Static/Dynamic	Off/Differential	Off, 50
HSUL18I/HSUL18II	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 50
LVCMOS25	GPIO, HSIO	Off/Static	Off/Down	Off, 120, 240
LVCMOS18/ LVCMOS15/ LVCMOS12	GPIO, HSIO	Off/Static	Off/Up/Down/ Thévenin	Off, 60, 120,240

2.14 ODT Value (ohm)

If ODT option is turned on, the ODT value can be set to any one of the values in the pull-down list. The ODT Value varies with different I/O standards. The following table lists acceptable values.

I/O Standard	Values
LVCMOS12 LVCMOS15 LVCMOS18 LVCMOS25 HSUL12I	120, 240. The default is 120.
SSTL15I SSTL15II	20, 30, 40, 60, 120. The default is 30.
SSTL135I SSTL135II	20, 30, 40, 60, 120. The default is 40.
SSTL18I SSTL18II	50, 75, 150. The default is 50.
LVSTL11I LVSTL11II	30, 34, 40, 48, 60, 80, 120, 240. The default is 60.
POD12I POD12II	34, 40, 48, 60, 80, 120, 240. The default is 40.

LVDS33 LVDS25 LVPECL33 LVPECL25 MINILVDS33 MINILVDS25 RSDS33 RSDS25 SLVSE15 SUBLVDS33 SUBLVDS25 LCMDS33 LCMDS25	100
HSTL15I HSTL15II HSUL18I HSUL18II HSTL12I HSTL12II HSTL135I HSTL135II	50

2.15 Slew

The slew rate is the amount of rise or fall time an input signal takes to get from logic low to logic high or vice versa. It is commonly defined to be the propagation delay between 10% and 90% of the signal's voltage swing. The PolarFire I/O Editor supports slew rate control in non-differential output mode. Turning the slew rate on results in faster slew rate, which improves the available timing margin, see *PolarFire FPGA Datasheet (to be released)* for the timing data. When slew rate is turned off, the device uses the default slew rate to reduce the impact of simultaneous switching noise (SSN). By default, the slew control is OFF.Not all I/O standards support the slew rate control.

Table 3 • **Slew Rate Control**

I/O Standards	Supported I/O Type	Slew Rate Control Options
LVTTL	GPIO (output only)	On (Default) or Off (on conditions)
LVCMOS25/LVCMOS33		
PCI		

Slew rate control is not available in PolarFire HSIO buffers. However, these buffers have built-in PVT-compensated slew rate controllers for optimized signal integrity

2.16 Output Drive (mA)

For LVCMOS, LVTTL, LVDS, and PPDS I/O standards, the PolarFire device has programmable output drive strength control to mitigate the effects of high signal attenuation caused by long transmission lines. Use the Output Drive (mA) field to set the Output Drive strength (mA). The output drive strength that can

be set is different with different I/O standards and can vary from 1 to 20 mA. Select the drive strength value from the list of valid values in the pull-down list.

Table 4 • **Programmable Drive Strength Control**

I/O Standards	Supported I/O Types	Drive Strength (mA)
LVTTL	GPIO (output only)	2, 4, 8, 12, 16, 20
LVCMOS33	GPIO (output only)	2, 4, 8, 12, 16, 20
LVCMOS25	GPIO (output only)	2, 4, 6, 8, 12, 16
LVDS25/LVDS33	GPIO (output only)	3, 3.5, 4, 6
RSDS33/RSDS25	GPIO (output only)	1.5, 2, 3
MINILVDS33/MINILVDS25	GPIO (output only)	3, 3.5, 4, 6
SUBLVDS33/SUBLVDS25	GPIO (output only)	1, 1.5, 2
PPDS33/PPDS25	GPIO (output only)	1.5, 2, 3
LVCMOS18	GPIO AND HSIO (output only)	2, 4, 6, 8, 10, 12
LVCMOS15	GPIO AND HSIO (output only)	2, 4, 6, 8, 10
LVCMOS12*	GPIO AND HSIO (output only)	2, 4, 6, 8, 10
*LVCMOS12 output drive strength of 10mA is supported only for HSIO		

2.17 Impedance (Ohm)

For voltage reference I/O standards, PolarFire I/Os provide the option to control the driver impedance for certain I/O standards: SSTL, HSUL, HSTL, POD, and LVSTL. Use the Impedance (Ohm) field in the I/O Editor to program the output impedance values. Note that the Impedance value is different with different I/O standards and can vary from 22 to 240 Ohm. Click on this field to open the pull-down list to see the valid values.

Table 5 • **Programmable Output Impedance Control**

I/O Standard	Supported I/O Types	Impedance (ohm)
SSTL25I	GPIO	48, 60, 80, 120. The default is 80.
SSTL25II	GPIO	34, 40, 48, 60. The default is 48.
SSTL18I	GPIO and HSIO	40, 48, 60, 80. The default is 60.
SSTL18II	GPIO and HSIO	30, 34, 40, 48. The default is 40.
SSTL15I	GPIO and HSIO	40, 48. The default is 40.
SSTL15II	GPIO and HSIO	27, 30, 34. The default is 34.
SSTL135I	HSIO	40, 48. The default is 40.

Table 5 • **Programmable Output Impedance Control *(continued)***

I/O Standard	Supported I/O Types	Impedance (ohm)
SSTL135II	HSIO	27, 30, 34. The default is 34
HSUL18I	GPIO and HSIO	34, 40, 55, 60. The default is 55.
HSUL18II	GPIO and HSIO	22, 25, 27, 30. The default is 25.
HSTL12I	GPIO and HSIO	50
HSTL12II	GPIO and HSIO	25
HSTL15I	GPIO and HSIO	34, 40, 50, 60. The default is 50.
HSTL15II	GPIO and HSIO	22, 25, 27, 30
HSTL135I	HSIO	34, 40, 50, 60. The default is 50.
HSTL135II	HSIO	22, 25, 27, 30. The default is 25.
HSUL12I	HSIO	34, 40, 48, 60, 80, 120. The default is 40.
POD12I	HSIO	40, 48, 60. The default is 48.
POD12II	HSIO	27, 30, 34. The default is 34.
LVSTL11I	HSIO	30, 34, 40, 48, 60, 80, 120, 240. The default is 40.
LVSTL11II	HSIO	30, 34, 40, 48, 60, 80, 120, 240. The default is 40.

2.18 Output Load (pF)

The Output Load indicates the output capacitance value based on the I/O standard. The default value is 65535 picofarads (pF). If necessary, you can double-click on the respective I/O port to change the output capacitance value to improve timing definition and analysis. Output capacitance affects output propagation delay.

SmartTime, Timing-driven layout and Backannotation automatically uses the modified delay model for delay calculations.

2.19 Source Termination (Ohm)

Near End termination for a differential output I/O.

The default is OFF.

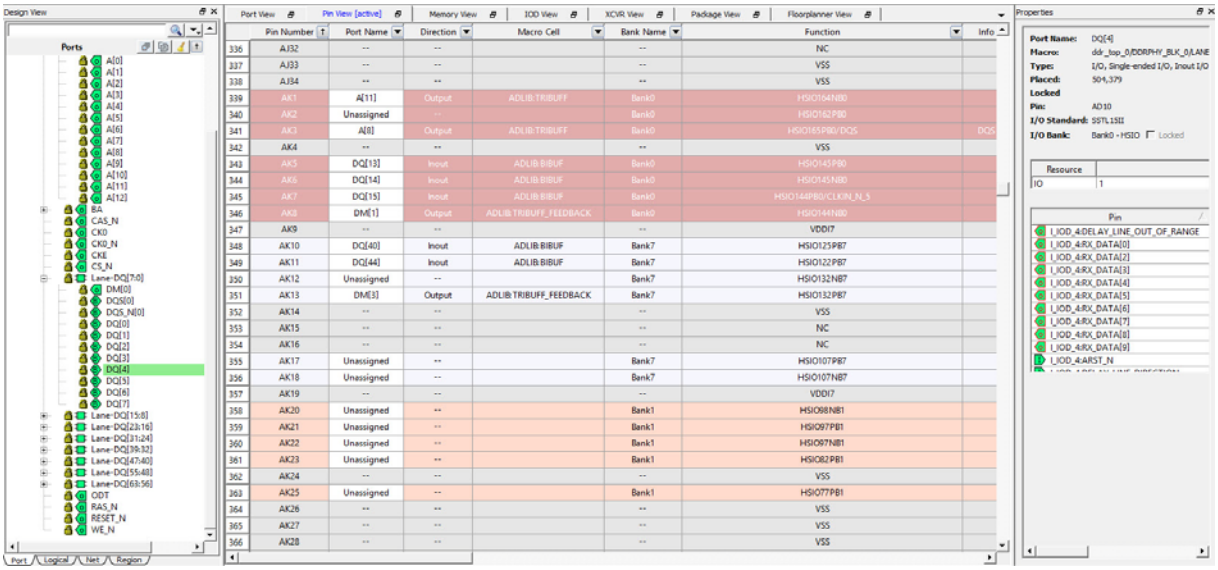
Direction: Output

3 Pin View

The Pin view displays the I/O Attributes of PolarFire I/O attributes in a spreadsheet-like format. Each row corresponds to an I/O macro (port) in the design, sorted by Pin number.The column headings specify the names of the I/O attributes in your design. The first four column headings are standard for all families so they will not change. For some I/O attributes, you will choose from a drop-down menu; for others, you might enter a value and for others, the field is read-only and not editable.

The display in the columns can be sorted alphabetically, numerically or filtered.

Figure 3 • **Pin View**



3.1 Pin Number

This is the read-only package pin number specific to the die and package of the PolarFire device.

3.2 Port Name

This is an editable field for the assignment of a port to that particular pin number. It contains a pull-down list of the assignable and available Ports for the pin. Select Unassigned to leave the pin unassigned.

3.3 Direction

Non-editable field that denotes Input, Output, or Inout.

3.4 Macro Cell

This is a Read-only field that identifies the name of the Macro cell associated with the Port.

3.5 Bank Name

This is a read-only field to identify the I/O bank the I/O pin is associated with. PolarFire devices may five, six, or eight I/O Banks (Bank 0 through Bank 7) user I/O banks, depending on the device size. Each pin is associated with an I/O bank. The I/O banks on the north side of the device support only HSIO. Each

I/O bank has dedicated I/O supplies and grounds. Each I/O within a given bank shares the same V_{DDI} power supply, and the same V_{REF} reference voltage. Only compatible I/O standards can be assigned to a given I/O bank.

3.6 Function

The function name identifies the functions of the pin/port. This is the same as what is listed in the Public Pin Assignment Table (PPAT) for the selected device and package. The PPAT for each PolarFire package are provided in the PolarFire_<package> Pinouts file on the PolarFire Documentation web page. For details, see the device datasheet of the die/package.

The function name may contain the following information:

- Type of I/O: GPIO or HSIO
- Special-purpose IOs: e.g. XCVR
- The I/O Bank Number
- Positive/Negative Pad of differential IOs
- VSS or Ground

3.7 Locked

Set this option to lock all I/O banks, so the I/O Bank Assigner cannot unassign and re-assign the technologies in the design.

3.8 User Reserved

For the I/O pin you want to reserve for use in another design, check the User Reserved checkbox to reserve it. When a pin is reserved, you cannot assign it to a port.

3.9 Dedicated

If checked, the pin is reserved for some special functionality, such as UJTAG, Power, XVCR Reference Clock, device reset, and clock functions.

3.10 Vref (Voltage Referenced)

Any PolarFire GPIO and HSIO pad on the device can be configured to act as an external V_{REF} to supply all inputs within a bank. Use this field to configure the I/O as V_{REF} to other I/Os. When an I/O pad is configured as voltage referenced, all I/O buffer modes and terminations on that pad are disabled.

3.11 User I/O Lock Down

If checked, the current pin assignment cannot be changed during layout.

3.12 I/O State in Flash Freeze Mode

By default, all the I/Os become tristated when the device goes into Flash*Freeze mode. You can override this default behavior by setting its value to one of the following two values:

- LAST_VALUE - When set to this value, it preserves the previous state of the I/O. This means the I/O remains in the same state in which it was functioning before the device went into Flash*Freeze mode.
- LAST VALUE_WP - When set to this value, it preserves the last value with weak pull-up.

3.13 Clamp Diode

PolarFire devices have internal PCI clamp diodes for both HSIO and GPIO. PCI clamp diodes help reduce the voltage level at the input, and are mainly used when the voltage overshoot exceeds the maximum allowable limit. If signaling levels of the receiver are greater than the V_{DDIx} of the bank, the clamp diode must be off to support hot-socketing insertion.

For GPIO, use this field to program the clamp diode to be ON or OFF.

For HSIO, the internal clamp diode is always on by default.

The following table lists the values for GPIO standards.

I/O Standard	Values
LVCMOS12, LVCMOS15, LVCMOS18, SSTL18I, SSTL18II, SSTL15I, SSTL15II, HSTL15I, HSTL15II, LVTTL, LVCMOS33, LVCMOS25, SSTL25I, SSTL25II, MIPI25	OFF, ON. The default is ON.
HSUL18I, HSUL18II, SLVSE15, MIPI12, PCI, SLVS33, HCSL33, MIPIE33, LVPECL33, LVPECL25, LVPECLE33, LVDS25, LVDS33, RSDS25, RSDS33, MINILVDS25, MINILVDS33, SUBLVDS25, SUBLVDS33, PPDS25, PPDS33, MLVDSE25, BUSLVDSE25, LCMDS33, LCMDS25	ON

3.14 Resistor Pull

Use this field to allow inclusion of a weak resistor for either pull-up or pull-down of the input buffer. The available options are None, Hold, Up (pull-up), or Down (pull-down). The default value is None, except when an I/O exists in the netlist as a port, is not connected to the core, and is configured as an output buffer. In that case, the default setting is for a weak pull-down.

Note: Not all I/O standards have a selectable resistor pull option.

3.15 Schmitt Trigger

PolarFire GPIO and HSIO can be configured as a Schmitt Trigger input. When enabled as such (YES), it exhibits a hysteresis that helps to filter out the noise at the receiver and prevents double-glitching caused by noisy input edges. Default value is OFF

For the following I/O standards, the values are OFF, ON.

I/O Standard	Values
GPIO	
LVCMOS25, LVCMOS33, LVTTL, PCI	OFF, ON
HSIO	
LVCMOS18, LVCMOS15	OFF, ON

For all other I/O standards, the value is OFF (Schmitt Trigger disabled).

3.16 Vcm Input Range

Values for all I/O standards are MID, LOW. The default is MID.

3.17 On-Die Termination (ODT)

ODT is an option used to terminate input signals. Terminating input signals helps to maintain signal quality, save board space, and reduces external component costs. In PolarFire FPGAs, ODT is available in receive mode and also in bidirectional mode when the I/O acts as an input. If ODT is not used or not available, the PolarFire I/O standards may require external termination for better signal integrity.

ODT can be a pull-up, pull-down, differential, or Thévenin termination with both static and dynamic control available, and is set using either the Libero SoC software I/O attribute editor or by using a PDC command.

In addition, ODT can be controlled dynamically for individual I/Os as well as for all I/Os in a lane simultaneously on a per-lane basis.

Table 6 • **ODT Support in GPIO and HSIO**

I/O Standards	I/O Types (Input Only)	ODT Control	ODT Type	ODT Value (ohm)
LVDS33/LVDS25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
RSDS33/RSDS25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
MINILVDS33/ MINILVDS25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
SUBLVDS33/ SUBLVDS25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
LVPECL33/ LVPECL25	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
SSTL18I/SSTL18II	GPIO, HSIO	Off/Static/Dynamic	Off/Thévenin	Off, 50, 75, 150
SSTL15I, SST15II	GPIO, HSIO	Off/Static/Dynamic	Off/Thévenin	Off, 20, 30, 40, 60, 120
RSDS33/RSDS25/	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	Off, 100
HSTL15I/HSTL15II	GPIO	Off/Static/Dynamic	Off/Differential	off, 50
HSUL18I/HSUL18II	GPIO, HSIO	Off/Static/Dynamic	Off/Differential	off, 50
LVCMOS25	GPIO, HSIO	Off/Static	Off/Down	Off, 120, 240
LVCMOS18/ LVCMOS15/ LVCMOS12	GPIO, HSIO	Off/Static	Off/Up/Down/ Thévenin	Off, 60, 120,240

3.18 ODT Value (ohm)

If ODT option is turned on, the ODT value can be set to any one of the values in the pull-down list. The ODT Value varies with different I/O standards.

Values vary depending on the I/O standard. The following table lists acceptable values.

I/O Standard	Values
LVCMOS12 LVCMOS15 LVCMOS18 LVCMOS25 HSUL12I	120, 240. The default is 120.
SSTL15I SSTL15II	20, 30, 40, 60, 120. The default is 30.
SSTL135I SSTL135II	20, 30, 40, 60, 120. The default is 40.

SSTL18I SSTL18II	50, 75, 150. The default is 50.
LVSTL11I LVSTL11II	30, 34, 40, 48, 60, 80, 120, 240. The default is 60.
POD12I POD12II	34, 40, 48, 60, 80, 120, 240. The default is 40.
LVDS33 LVDS25 LVPECL33 LVPECL25 MINILVDS33 MINILVDS25 RSDS33 RSDS25 SLVSE15 SUBLVDS33 SUBLVDS25 LCMDS33 LCMDS25	100
HSTL15I HSTL15II HSUL18I HSUL18II HSTL12I HSTL12II HSTL135I HSTL135II	50

3.19 Slew

The slew rate is the amount of rise or fall time an input signal takes to get from logic low to logic high or vice versa. It is commonly defined to be the propagation delay between 10% and 90% of the signal's voltage swing. The PolarFire I/O Editor supports slew rate control in non-differential output mode. Turning the slew rate on results in faster slew rate, which improves the available timing margin, see DS0141: PolarFire FPGA Datasheet for the timing data. When slew rate is turned off, the device uses the default slew rate to reduce the impact of simultaneous switching noise (SSN). By default, the slew control is OFF.Not all I/O standards support the slew rate control.

Table 7 • **Slew Rate Control**

I/O Standards	Supported I/O Type	Slew Rate Control Options
LVTTL	GPIO (output only)	On (Default) or Off (on conditions)
LVCMOS25/LVCMOS33		
PCI		

Slew rate control is not available in PolarFire HSIO buffers. However, these buffers have built-in PVT-compensated slew rate controllers for optimized signal integrity

3.20 Output Drive (mA)

For LVCMOS, LVTTL, LVDS, and PPDS I/O standards, the PolarFire device has programmable output drive strength control to mitigate the effects of high signal attenuation caused by long transmission lines. Use the Output Drive (mA) field to set the Output Drive strength (mA). The output drive strength that can be set is different with different I/O standards and can vary from 1 to 20 mA. Select the drive strength value from the list of valid values in the pull-down list.

Table 8 • **Programmable Drive Strength Control**

I/O Standards	Supported I/O Types	Drive Strength (mA)
LVTTL	GPIO (output only)	2, 4, 8, 12, 16, 20. The default is 8.
LVCMOS33	GPIO (output only)	2, 4, 8, 12, 16, 20. The default is 8.
LVCMOS25	GPIO (output only)	2, 4, 6, 8, 12, 16. The default is 8.
LVDS25/LVDS33	GPIO (output only)	3, 3.5, 4, 6. The default is 6.
RSDS33/RSDS25	GPIO (output only)	1.5, 2, 3. The default is 3.
MINILVDS33/MINILVDS25	GPIO (output only)	3, 3.5, 4, 6. The default is 6.
SUBLVDS33/SUBLVDS25	GPIO (output only)	1, 1.5, 2. The default is 2.
PPDS33/PPDS25	GPIO (output only)	1.5, 2, 3. The default is 3.
LVCMOS18	GPIO AND HSIO (output only)	2, 4, 6, 8, 10, 12. The default is 8.
LVCMOS15	GPIO AND HSIO (output only)	2, 4, 6, 8, 10. The default is 8.
LVCMOS12*	GPIO AND HSIO (output only)	2, 4, 6, 8, 10. The default is 8.
*LVCMOS12 output drive strength of 10mA is supported only for HSIO		

3.21 Impedance (Ohm)

For voltage reference I/O standards, PolarFire I/Os provide the option to control the driver impedance for certain I/O standards: SSTL, HSUL, HSTL, POD, and LVSTL. Use the Impedance (Ohm) field in the I/O Editor to program the output impedance values. Note that the Impedance value is different with different I/O standards and can vary from 22 to 240 Ohm. Click on this field to open the pull-down list to see the valid values.

Table 9 • **Programmable Output Impedance Control**

I/O Standard	Supported I/O Types	Impedance (ohm)
SSTL25I	GPIO	48, 60, 80, 120. The default is 80.
SSTL25II	GPIO	34, 40, 48, 60. The default is 48.
SSTL18I	GPIO and HSIO	40, 48, 60, 80. The default is 60.
SSTL18II	GPIO and HSIO	30, 34, 40, 48. The default is 40.

Table 9 • **Programmable Output Impedance Control *(continued)***

I/O Standard	Supported I/O Types	Impedance (ohm)
SSTL15I	GPIO and HSIO	40, 48. The default is 40.
SSTL15II	GPIO and HSIO	27, 30, 34. The default is 34.
SSTL135I	HSIO	40, 48. The default is 40.
SSTL135II	HSIO	27, 30, 34. The default is 34
HSUL18I	GPIO and HSIO	34, 40, 55, 60. The default is 55.
HSUL18II	GPIO and HSIO	22, 25, 27, 30. The default is 25.
HSTL12I	GPIO and HSIO	50
HSTL12II	GPIO and HSIO	25
HSTL15I	GPIO and HSIO	34, 40, 50, 60. The default is 50.
HSTL15II	GPIO and HSIO	22, 25, 27, 30
HSTL135I	HSIO	34, 40, 50, 60. The default is 50.
HSTL135II	HSIO	22, 25, 27, 30. The default is 25.
HSUL12I	HSIO	34, 40, 48, 60, 80, 120. The default is 40.
POD12I	HSIO	40, 48, 60. The default is 48.
POD12II	HSIO	27, 30, 34. The default is 34.
LVSTL11I	HSIO	30, 34, 40, 48, 60, 80, 120, 240. The default is 40.
LVSTL11II	HSIO	30, 34, 40, 48, 60, 80, 120, 240. The default is 40.

3.22 Output Load (pF)

The Output Load indicates the output capacitance value based on the I/O standard. The default value is 65535 picofarads (pF). If necessary, you can double-click on the respective I/O port to change the output capacitance value to improve timing definition and analysis. Output capacitance affects output propagation delay.

SmartTime, Timing-driven layout and Backannotation automatically uses the modified delay model for delay calculations.

3.23 Source Termination (Ohm)

Near End termination for a differential output I/O.

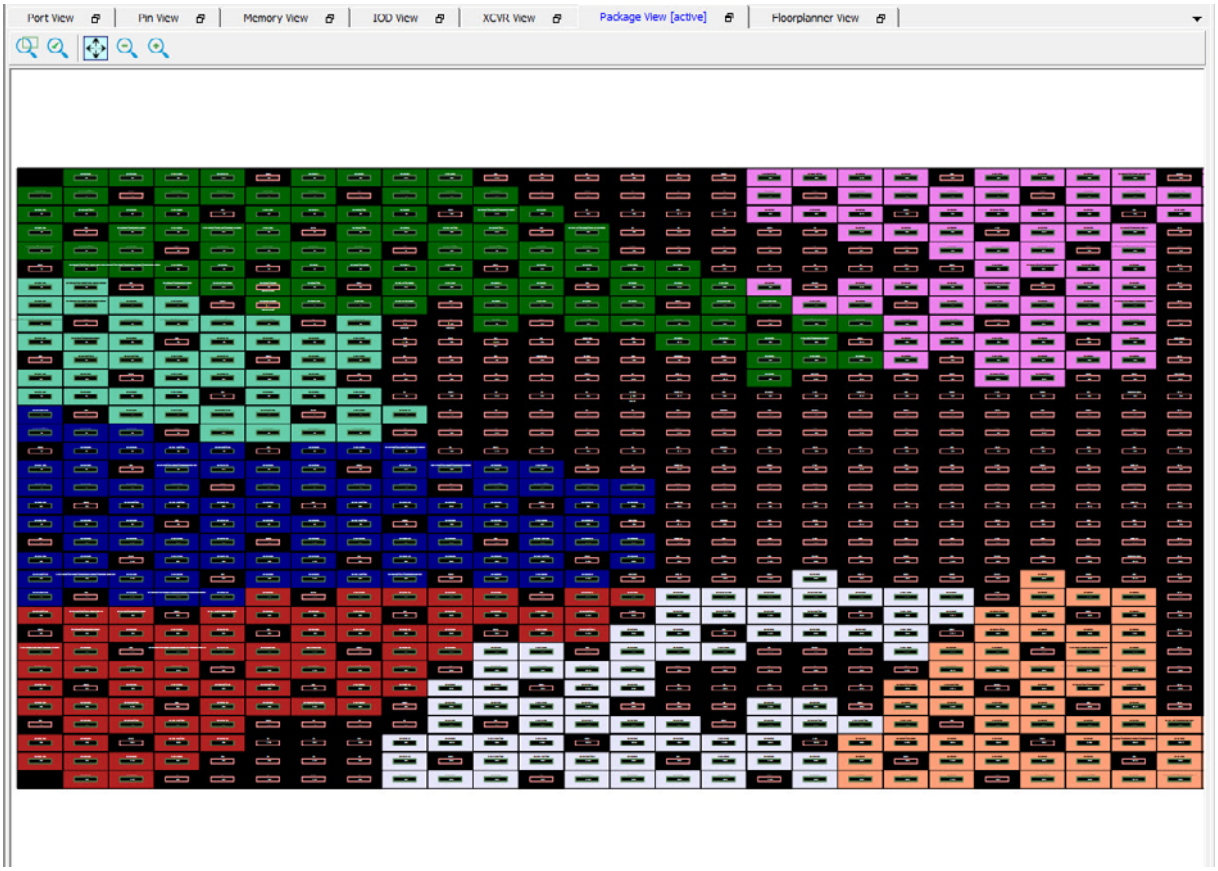
The default is OFF.

Direction: Output

4 Package View

The Package View displays the Package pin views of the particular die/package of the PolarFire device.The color for the display of the pins are determined by the settings in the Display Options pane. Figure 4 · Package View shows the regular pins in green, special pins in blue, reserved pins in red and unconnected pins in grey.

Figure 4 • **Package View**



5 Interface-Specific I/Os and Views

The PolarFire architecture is designed and optimized to support Memory Interface, IOD interface and Transceiver interface. The PolarFire I/O Editor provides three special views specifically for I/O assignments of these interfaces.

For optimal QOR (Quality of Result) and timing performance, the architecture of the PolarFire silicon requires the Memory Interface, IOD Interface and Transceiver Interface be placed in specific and pre-defined locations of the chip. Assignment of these interfaces are checked against PolarFire DRC rules and illegal assignments are flagged.

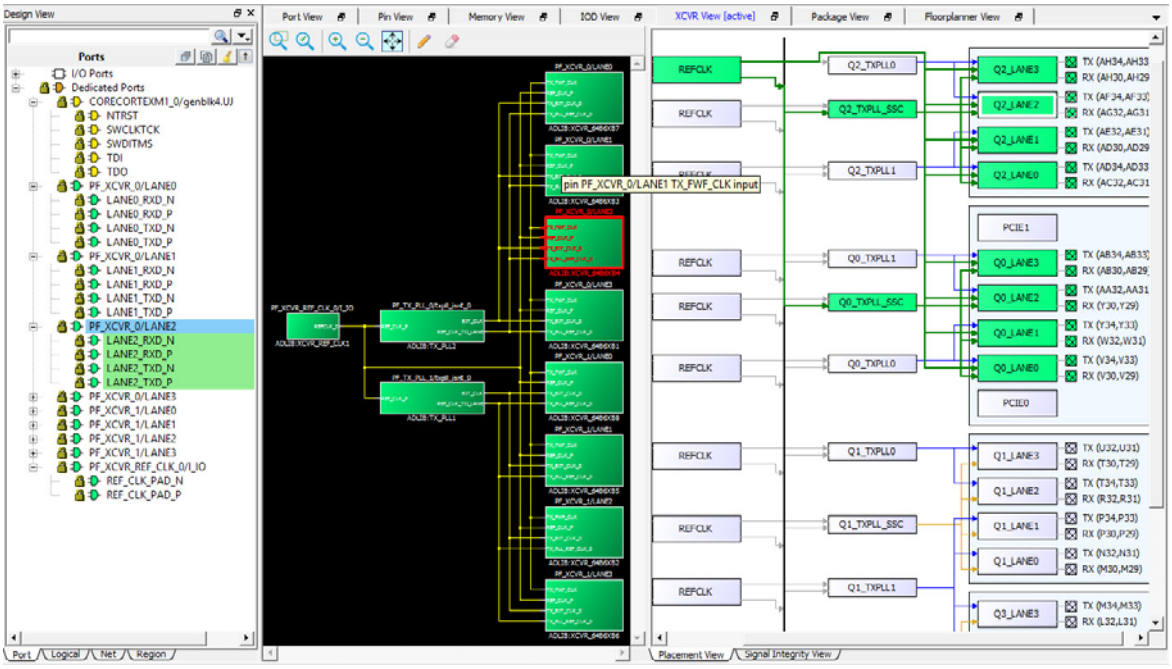
The PolarFire I/O Editor is a Graphical User Interface (GUI) tool designed to make Interface I/O pin assignments graphically and user-friendly, as an alternative to writing PDC commands. When the pin assignment is committed and saved in I/O Editor, a PDC file is created. This PDC file can then be passed to the Place and Route tool as a Physical Design Constraint.

5.1 Interface-Specific I/O Views

In addition to the Pin view, Port view and Package view, the PolarFire I/O Editor provides three views specific to PolarFire-supported interfaces I/Os:

- Memory View - for I/O pin assignments of Memory Interfaces such as DDR2/3/4,LPDDR2/3, QDR, and RLDRAMII.
- XCVR View - Presents a physical view of the Transceiver connectivity, including Transceiver lanes, and Reference Clock (REFCLK), and TransmitPLL lines.
- IOD Lane Controller View - Presents the I/O Digital block view, used for non-memory interfaces using the FPGA I/Os.

Figure 5 • **I/O Editor - XCVR View**



6 Memory Interface View

The Memory Interface view presents a spreadsheet-like view of the I/Os available in the PolarFire silicon for different Memory Interface types.

6.1 Memory Type

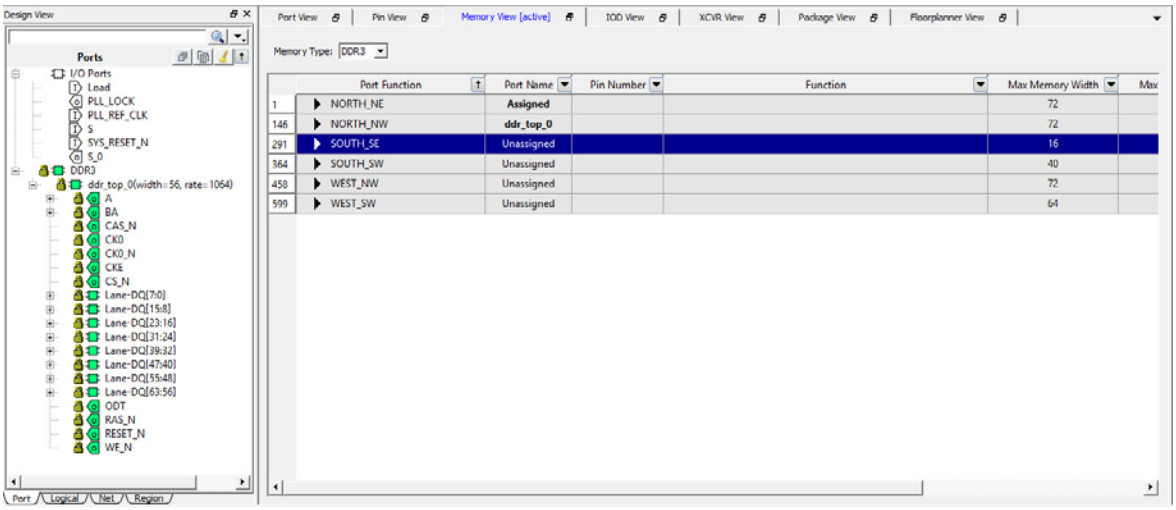
The supported Memory Interface types include:

- DDR2
- DDR3
- DDR4
- LPDDR2
- LPDDR3
- QDRII+
- RLDRAMII
- SDR

Click the pull-down menu to select the type of Memory Interface used in the design. Only the specific type of memory used in the design are displayed in the pull-down list.

The Ports view also displays the memory width and data rate of the DDR instance in the design (if it exists in the design) in the top left row under the Port Name column, as shown in Figure 6.

Figure 6 • **Memory Interface Type Menu**



6.2 Edge_Anchors For Memory Placement

The PolarFire silicon architecture requires the Memory Interface be placed in specific and pre-defined locations of the chip to achieve optimal QOR (Quality of Result) and Timing Performance. These specific location are called Edge_Anchors and are used to identify the specific location in the PolarFire chip for optimal Memory Interface I/O placement. See the PolarFire DDR Memory User Guide for a mapping of DDR memory interface types to Edge_Anchor locations. The list of Edge_Anchors are:

- NORTH_NE
- NORTH_NW
- SOUTH_SE
- SOUTH_SW

- WEST_NW
- WEST_SW

The ports for each Edge_Anchor is represented by a different color for easy identification. The list of possible Edge_Anchors is context-sensitive to the Memory Interface type and represents the legal and optimal locations for the specific Memory Interface type. The list of Edge_Anchors for DDR4, for example, is different from the list for DD2/DDR3. DDR4 has fewer locations (Edge_Anchors) for I/O placement than DDR2/DD3.

6.3 Memory Interface View Columns

The Memory Interface view detects the type of Memory Interface in the design and presents the ports in the Ports View. The Memory Interface View displays the following I/O information in the view. Each of the column can be sorted (ascending/descending order) or filtered.

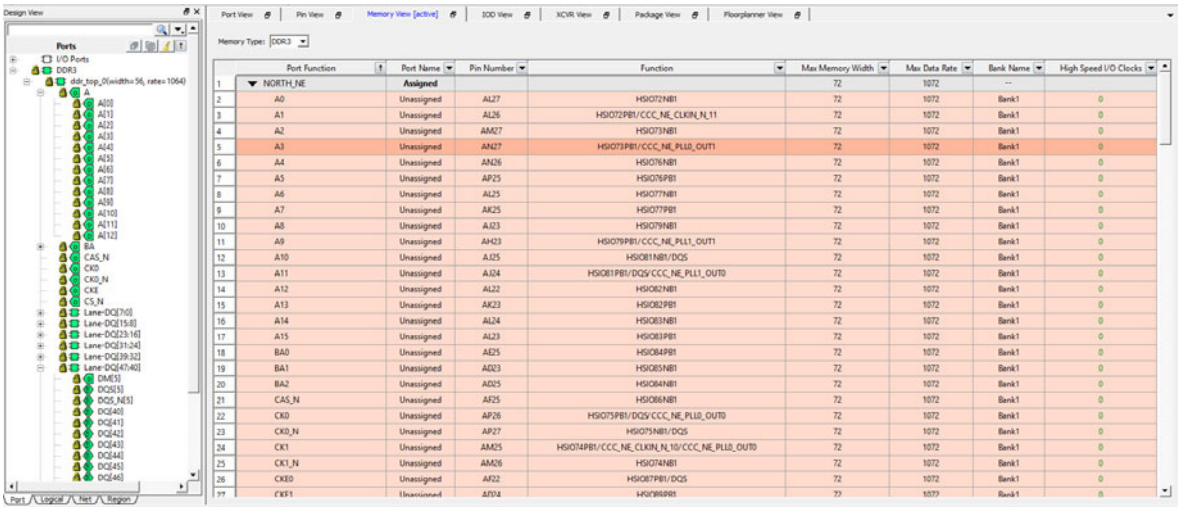
- Port Function - the formal port name of the Memory Interface. The ports specific to the memory interface type are loaded into the Port view.
- Port Name - the port name of the Memory Interface instance in the design.
- Pin Number - the package pin number assigned to the port of the Memory Interface
- Function - A more descriptive function name of the Port which identifies the type of I/O (e.g. HSIO for High-speed I/Os or GPIO (General-purpose IO)
- Max Memory Width - the maximum memory width of the DDR. This is a fixed read-only value specific to the Edge_Anchor and is different with different Edge_Anchors.
- Max Data Rate - the maximum data rate in Mbps. This is a fixed read-only value specific to the Edge_Anchor and is different with different Edge_Anchors.

Note: When making DDR placement, refer to the memory width and data rate of the DDR Memory used in the design (as displayed in the Ports View). Make sure that the Edge_Anchor location where you want to place the DDR memory can accommodate the DDR memory in terms of the memory width and the data rate. This will avoid invalid placement.

- Bank Name - the I/O bank name of the port
- High-speed I/O Clocks - specifies the number of High Speed I/O clocks

The Pin Number and Function are the same as what are listed in the Public Pin Assignment Table (PPAT) for the selected device and package. The PPAT for each PolarFire package are provided in the PolarFire_<package> Pinouts file on the PolarFire Documentation web page.

Figure 7 • **Memory Interface View**



6.4 Making I/O Assignments

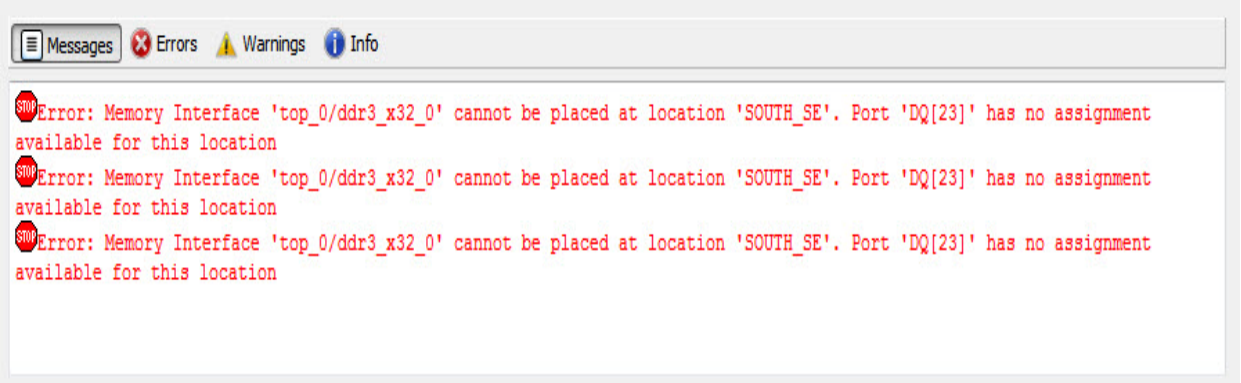
To make I/O assignment for the Memory Interface instance in the design:

1. Select the Memory Interface type from the drop-down menu.
2. From the Ports tab in the Design Tree View, drag the Memory Interface instance and let the mouse hover over one of the Edge_Anchor locations available for the Memory Interface type. A tooltip reports whether it is a legal or illegal location for the Interface instance.
3. Drop the Interface instance into a legal Edge_Anchor location.

   Notes: DRC rules are enforced. Drag-and-drop I/O placement that violates the DRC rules are reported in the Log window. For Memory Interface, the DRC checks the Data Width and the Data Rate compliance*. If the specific location cannot accommodate the Data Width or the Data Rate of the Memory Interface, no I/O assignment is made. An error is reported in the Log Window with a message that explains why the assignment is not accepted. In Figure 8 · DRC Checks In Log Window, the DRC error message reports that the ddr3 instance requires 64 ports but the SOUTH_SE location can accommodate only 58 pins.

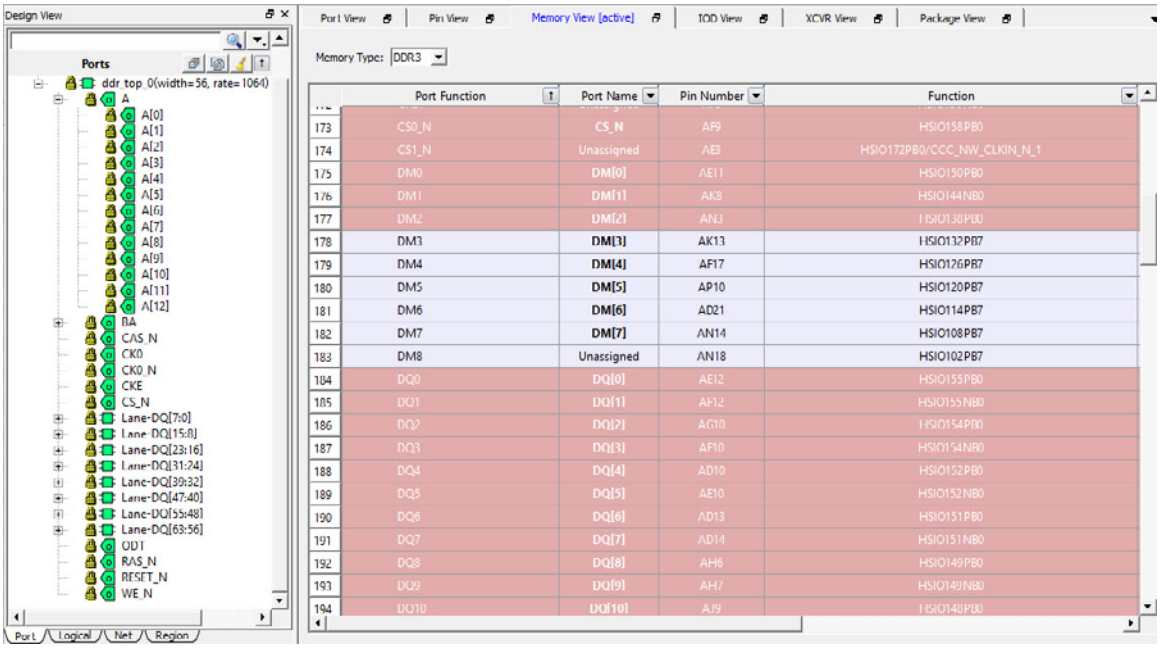
Note:*Data Rate compliance will be enforced in a later release.

Figure 8 • **DRC Checks In Log Window**



4. Check that no DRC error messages are reported in the Log window and the I/O assignments are accepted (Figure 9 · Memory Interface Assignments Accepted). The Lock icon in the Ports tab indicates that the I/O assignment is accepted and locked.

Figure 9 • **Memory Interface Assignments Accepted**



6.5 IO_PDC File

When the I/O assignment is committed and saved in the I/O Editor, the assignment is saved in a PDC file in the <project_folder/constraints/io/user.pdc file. The PDC file contains set_io commands on each of the the DDR Memory Interface I/O.

Figure 10 • **PDC File Generation after Memory Interface I/O Assignment in I/O Editor**

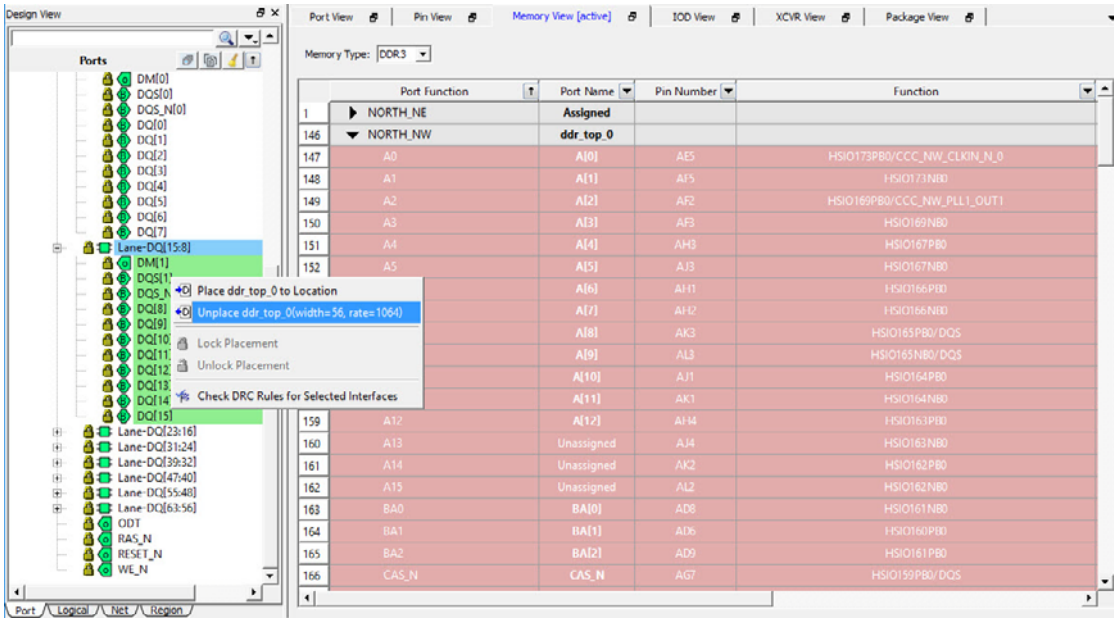
```
set_io -port_name {DQ[24]}  \
    -pin_name AG11          \
    -fixed true             \
    -ODT_VALUE 60           \
    -DIRECTION INOUT


set_io -port_name {DQ[25]}  \
    -pin_name AH11          \
    -fixed true             \
    -DIRECTION INOUT


set_io -port_name {DQ[26]}  \
    -pin_name AG12          \
    -fixed true             \
    -DIRECTION INOUT


set_io -port_name {DQ[27]}  \
    -pin_name AH12          \
    -fixed true             \
    -DIRECTION INOUT


set_io -port_name {DQ[28]}  \
    -pin_name AJ10          \
    -fixed true             \
    -DIRECTION INOUT


set_io -port_name {DQ[29]}  \
    -pin_name AJ11          \
    -fixed true             \
    -DIRECTION INOUT
```

6.6 Removing I/O Assignments

To remove a DDR Memory Interface I/O assignment:

1. Select the Port tab in the Design Tree view.
2. Right-click the Memory Interface in the Design Tree view.
3. Select Unplace <memory_interface_name>

Figure 11 • **Removing Memory Interface I/O Assignment**



7 XCVR View

The XCVR View allows the user to make assignments for Transceiver Lanes, Reference Clocks and Transmit PLLs. It presents the following views:

- A schematic view of the Reference Clock (REFCLK), the TransmitPLL and the Transceiver Lanes they drive (Figure 12 · XCVR Interface - Schematic View).
- A graphical placement view of the REFCLK, its connection from the PADS, to the TransmitPLL, to the Transceiver Lanes.(Figure 13 · XCVR Interface - Graphical Placement View).
- A Signal Integrity View for a Transceiver Lane, showing TX Emphasis Amplitude, TX Impedance, TX Transmit Common Mode Adjustment, RX and TX Polarity, RX Insertion Loss, RX CTLE, RX Termination, RX P/N Board Connection, and RX Loss of Signal Detector (Low and High) (Figure 14 · I/O Editor - XCVR View - Signal Integrity View).

Figure 12 • **XCVR Interface - Schematic View**

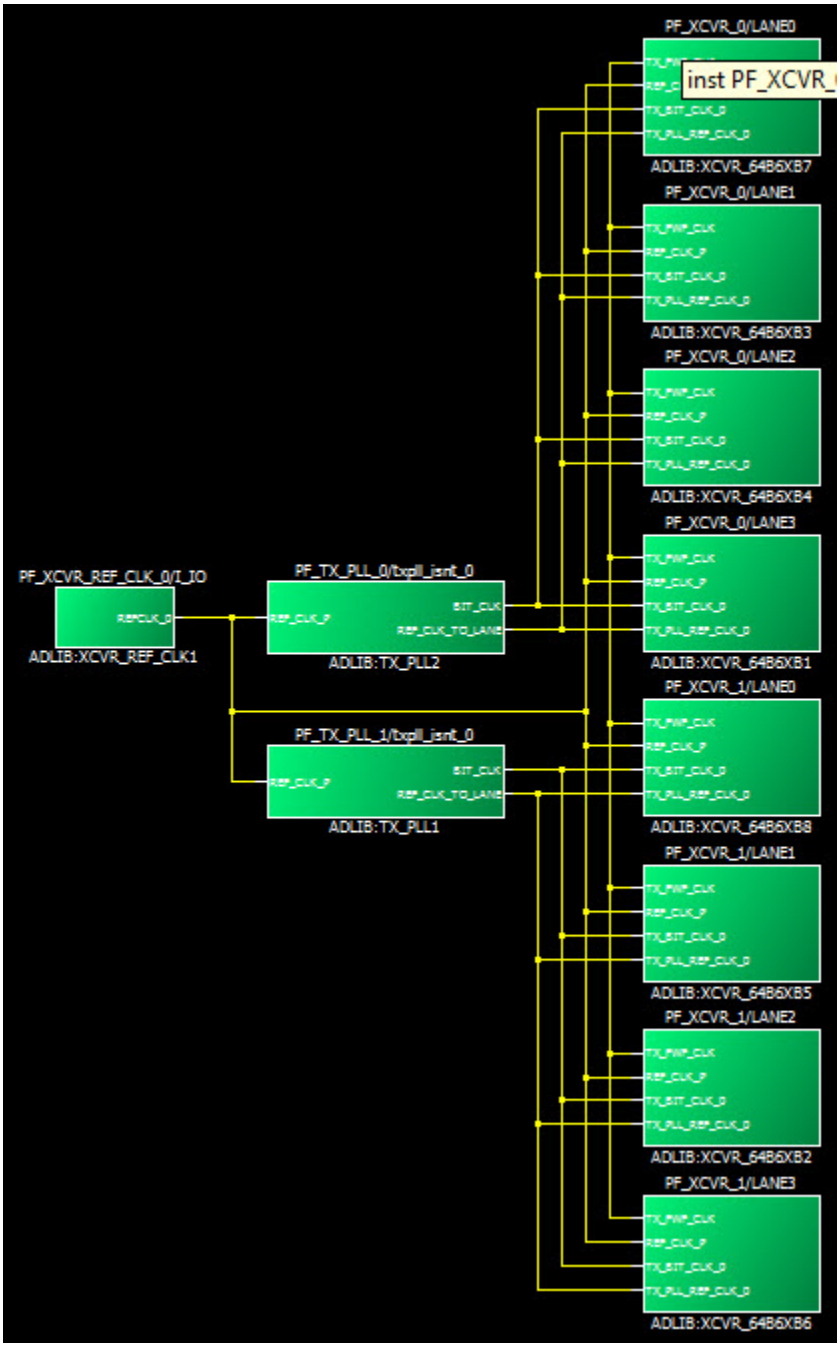


Figure 13 • **XCVR Interface - Graphical Placement View**

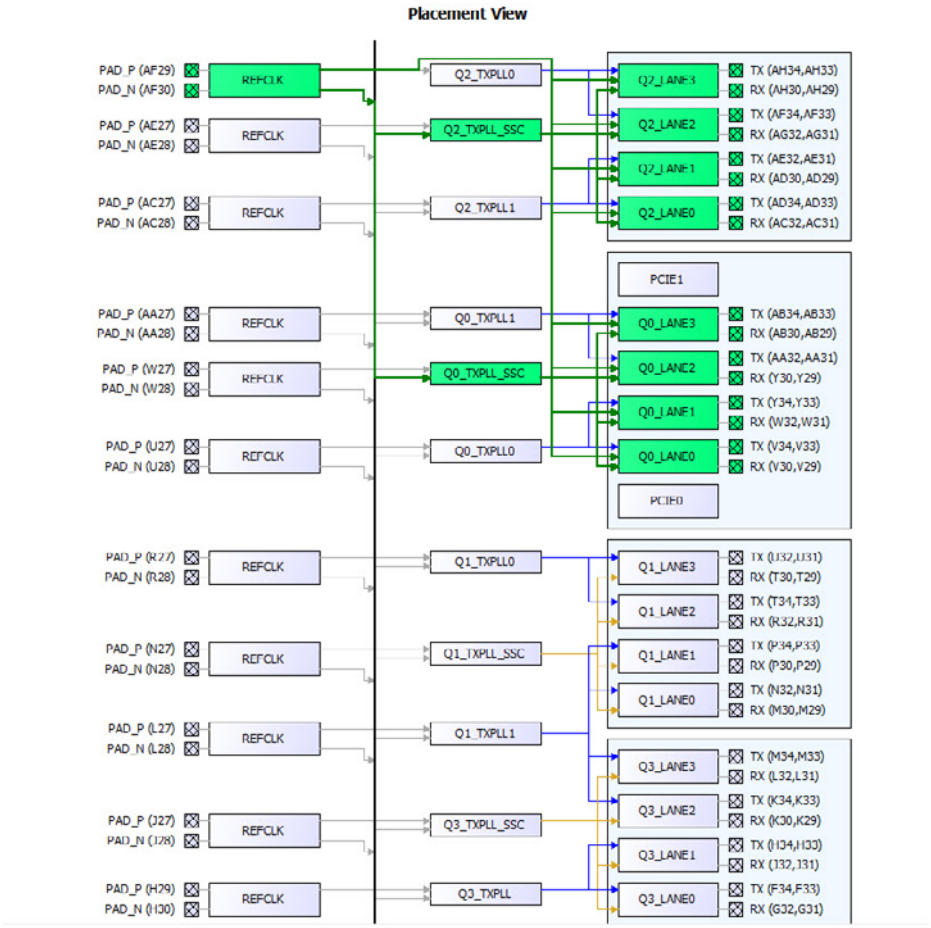
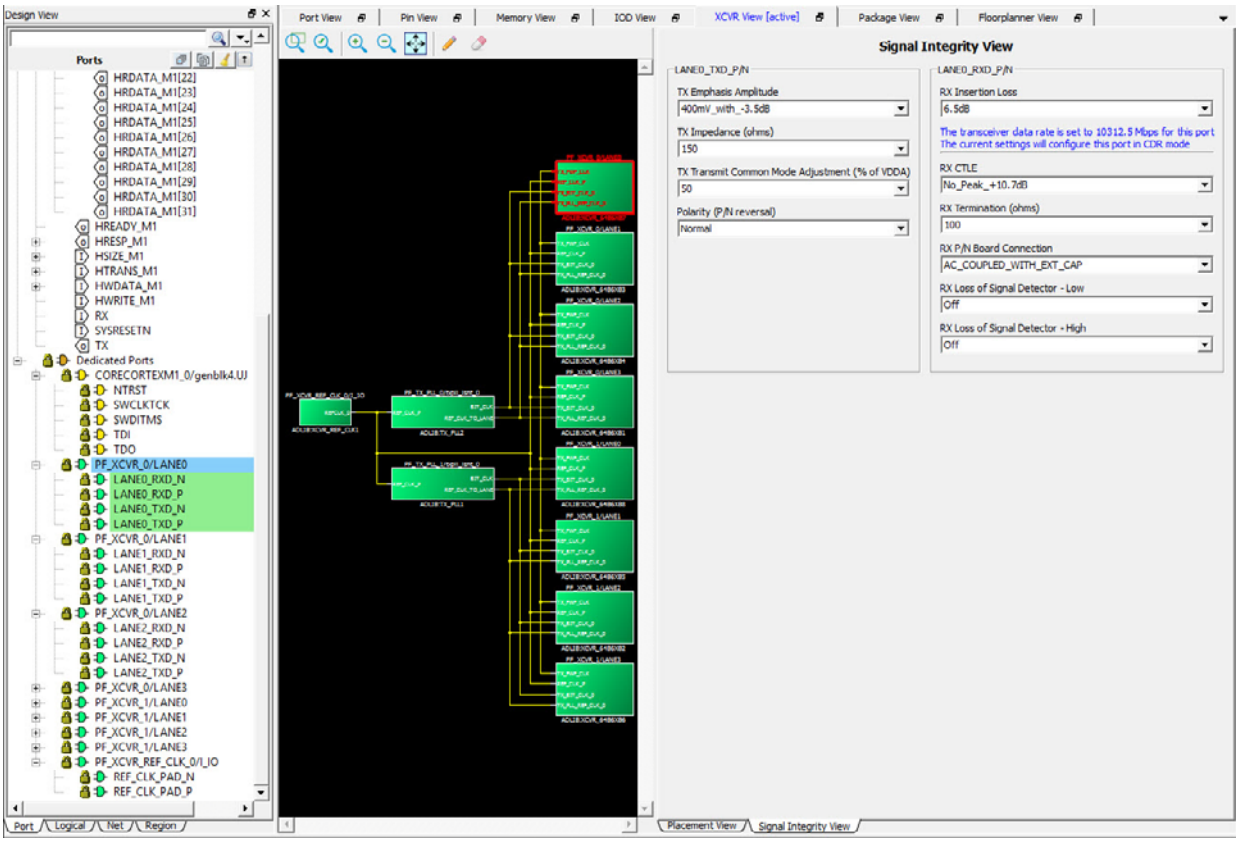


Figure 14 • **I/O Editor - XCVR View - Signal Integrity View**



The Signal Integrity View for a Transceiver Lane shows the following:

- TX Emphasis Amplitude
- TX Impedance
- TX Transmit Common Mode Adjustment
- RX and TX Polarity, RX Insertion Loss, RX CTLE
- RX Termination
- RX P/N Board Connection
- RX Loss of Signal Detector (Low and High)

7.1 XCVR Interface I/O Assignment

To make XCVR Interface I/O assignment, use the XCVR view in the PolarFire I/O Editor to make assignment in this order:

1. Transceiver Lanes
2. TX PLL
3. REFCLK

7.2 Direct Versus Cascaded Connection

The PolarFire XCVR reference clock network provides rich connectivity to the TX_PLL and Transceiver lanes. The connectivity allows the user to share common reference clock inputs to reduce fanout buffers on the board and reduce costs.

There are two types of connections between the reference clock and the TX _PLL and Transceiver lanes: Direct Connection and Cascaded Connection.

Direct connections are used when the reference clock pin and the TX_PLL or the Transceiver lanes are in the same Quad location.

Cascaded connections are used when the reference clock pin and the TX_PLL or the Transceiver lanes are not in the same quad location. Cascade connections are only available going from the top of the device towards the bottom.

The cascaded connection is denoted in the XCVR view by the black vertical line down the middle of the placement view.

Note: A REFCLK can connect to all the lanes beside or below it in any quad (down the cascade path) but not those above it (up the cascade path).

The red lines denote cascaded REFCLK connection to the TX_PLL and the Transceiver lanes in the quad.

Connection/Assignment up the Cascade path (from REFCLK to TX_PLL and Transceiver lanes which are above the REFCLK) are illegal and indicated by red lines in the XCVR view.

Each Reference Clock (REFCLK) has a direct dedicated connection to its corresponding TX_PLL and to the lane that the TX_PLL drives in the same quad.

Selecting a dedicated connection or a cascaded connection depends on the trade-off you want to make. A direct dedicated connection from the REFCLK to the TX_PLL gives better signal integrity for the Transceiver whereas a cascaded connection reduces external components and reduces overall power.

Figure 15 • **Direct Dedicated Path and Cascade Path**

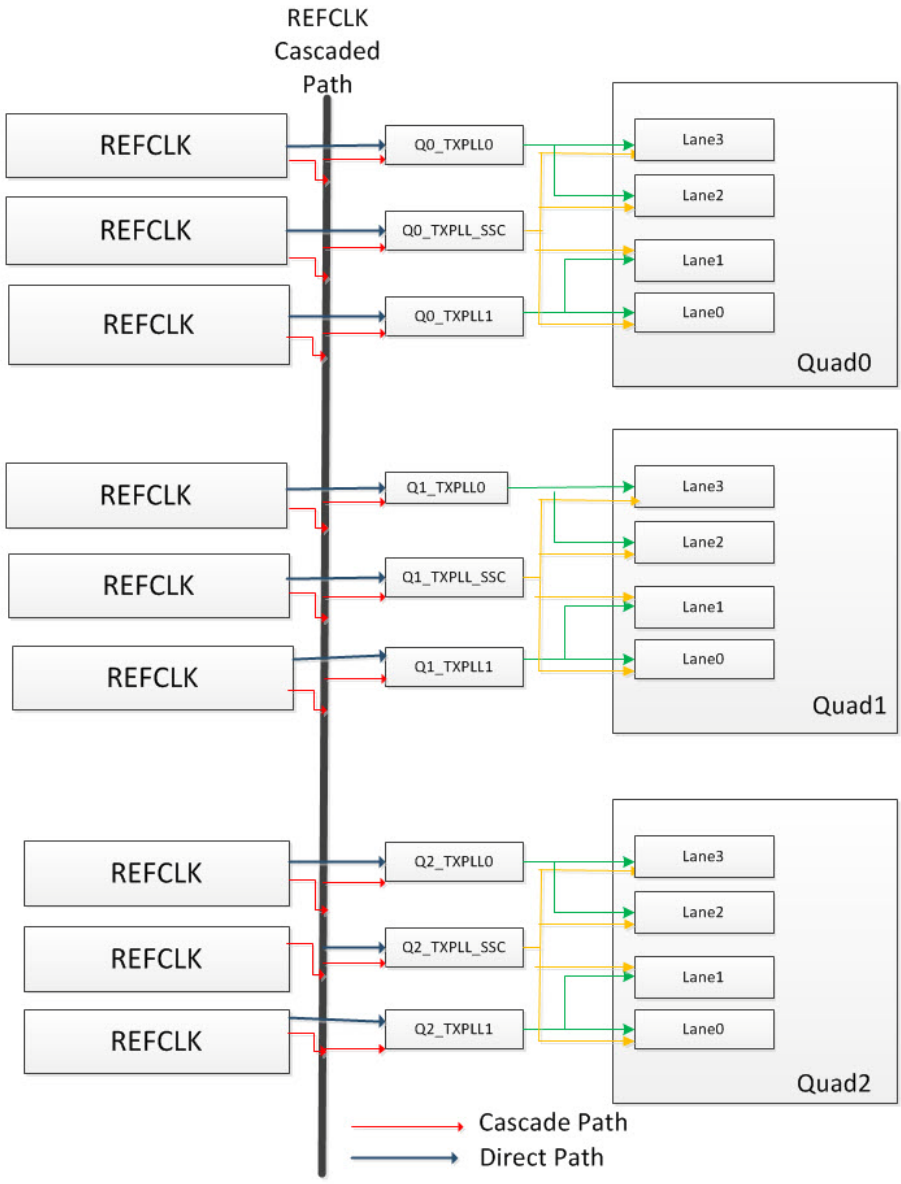
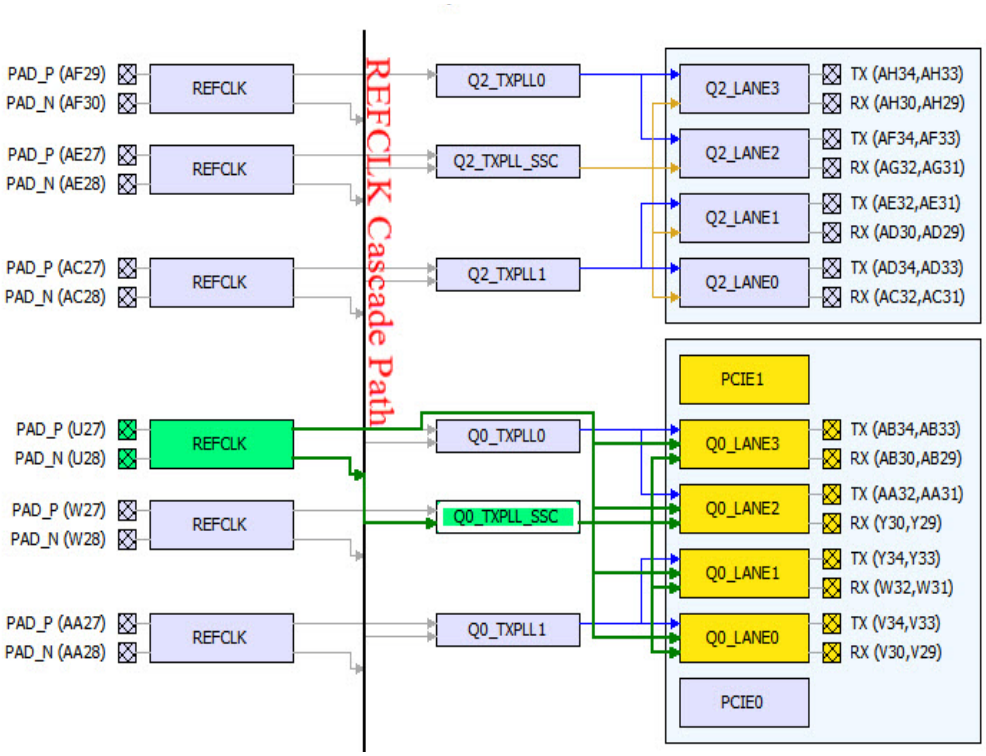


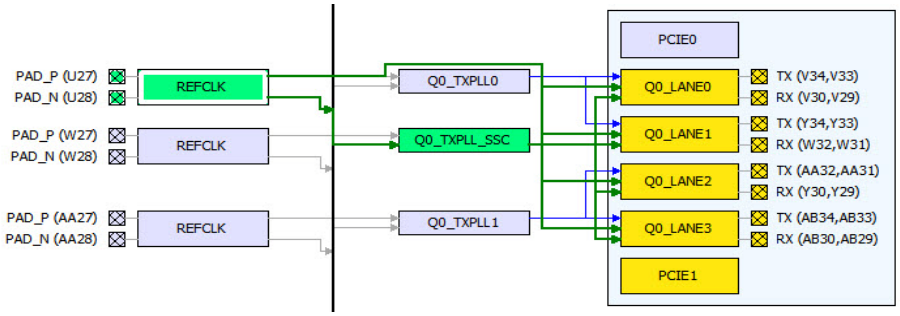
Figure 16 • **XCVR View**



7.3 Reference Clock (REFCLK) I/O Assignments

To make I/O assignments, click and drag the REFCLK pin from the Schematic View to the pin location you desire in the Graphical Placement View. If the assignment is legal (no DRC violations), green lines appear to denote the accepted connection between the REFCLK pin through the Q(x)_TXPLL_SSC to the Transceiver lanes.

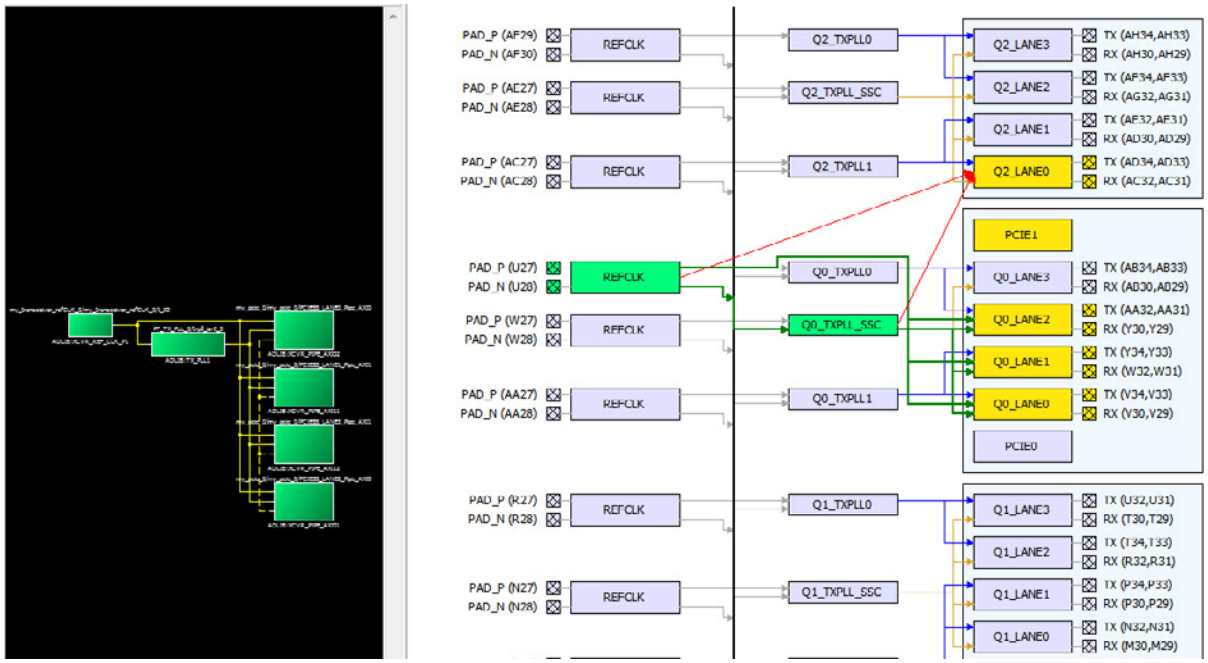
Figure 17 • **Legal and Accepted Reference Clock I/O Assignment**



If the I/O assignment violates the DRC rule, the assignment is not accepted. Red arrows denotes DRC violations.Figure 18 · Illegal I/O Assignment shows two illegal assignments:

- From the Reference Clock (REFCLK) to the Lanes (Red arrow from REFCLK to the Q2_Lane0)
- From the Transmit PLL to the lanes (Red arrow from TXPLL_SSC to Q2_Lane0)

Figure 18 • **Illegal I/O Assignment**



An error message appears in the Log window to identify the DRC rules violated. In this case, there is no feasible dedicated connection from the REFCLK to the Lane and from the Transmit PLL to the Lanes.

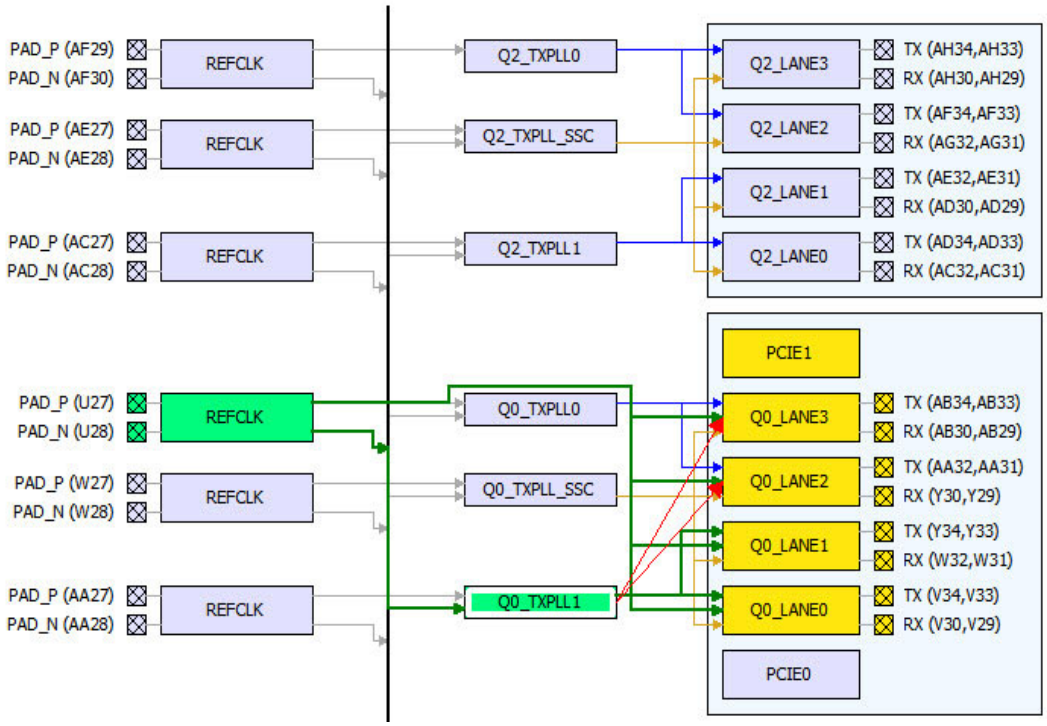
Figure 19 • **Log Window Message**

Notes: I/O assignments can be made for REFCLK, TXPLL and Transceiver Lanes for all Transceiver protocols except the PCIe Protocol. For the PCIe Protocol, Transceiver Lanes are assigned to pre-defined locations and cannot be removed.

7.4 Transmit PLL Assignment

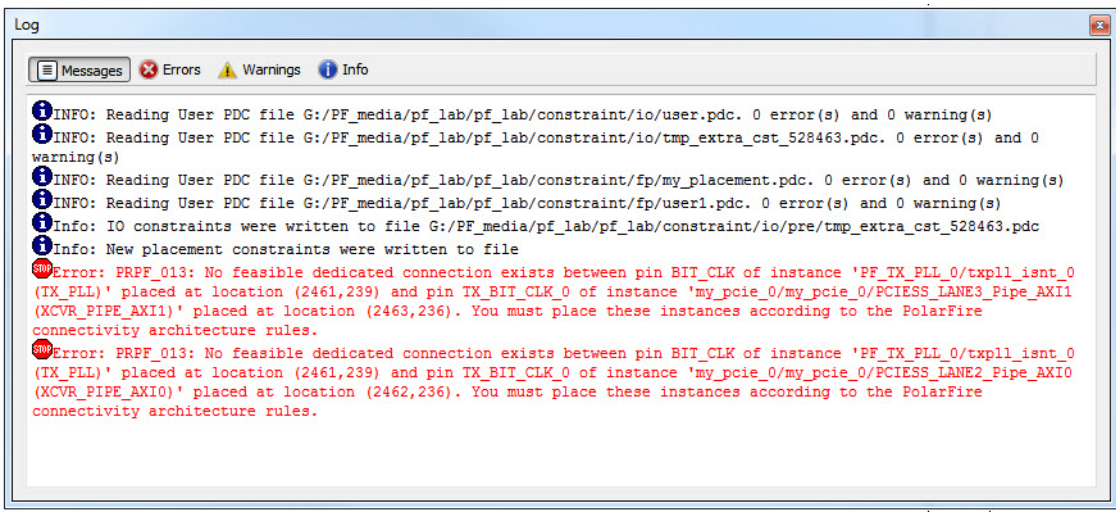
Drag and drop the Transmit PLL instance into the desired location. Illegal locations are flagged with error messages in the Log window and the illegal connections are indicated by red lines.

Figure 20 • **Illegal Transmit PLL to Lane Assignment**



The Log window displays two error messages about the illegal assignments, one for each illegal connection. In this case, the assignment is illegal because there are no feasible dedicated connections.

Figure 21 • **Log Window**



7.5 Placement DRC Rules

The I/O Editor enforces the DRC rules when Transceivers are placed. Any illegal connection is highlighted as a red line in the Placement View and a corresponding message is displayed in the Log window.

Lane assignments are always legal. DRC rules are enforced for the following:

- Connection from Transmit PLL (TXPLL) to the Lanes

- Connection from the Reference Clock (REFCLK) to the Transmit PLL (TXPLL)
- Connection from the Reference Clock (REFCLK) to the Lanes

7.5.1 DRC - TXPLL to LANES Connectivity

1. A TXPLL_SSC can connect to all the lanes of a quad (shown in brown lines in the Placement View).

Figure 22 • **TXPLL Connection To All Four Lanes Before Placement**

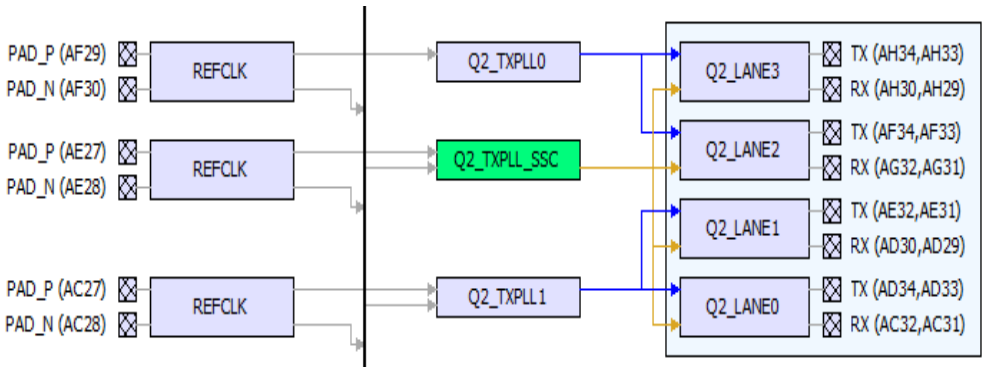
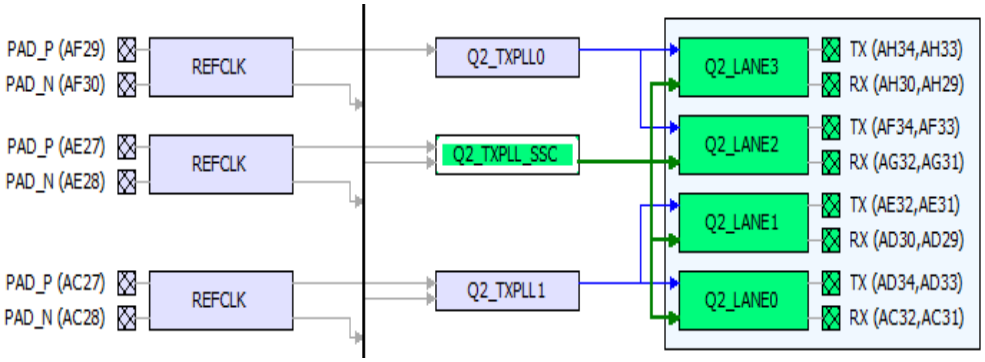


Figure 23 • **TXPLL Connection To All Four Lanes After Placement**



2. A TXPLL (non-SSC) can connect to two lanes beside it normally (shown in blue lines in the Placement View)

Figure 24 • **TXPLL Connection To Two Lanes (Before Placement)**

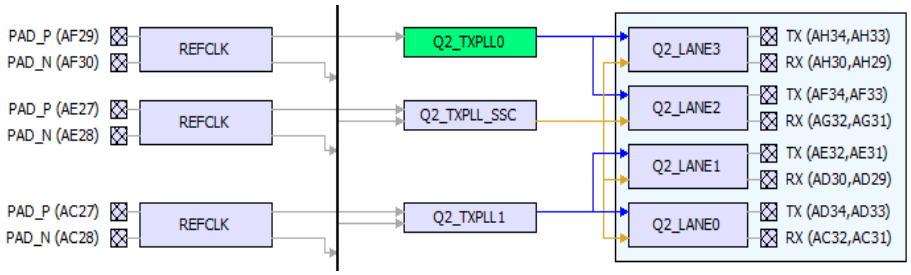


Figure 25 • **TXPLL Connection To Two Lanes (After Placement)**

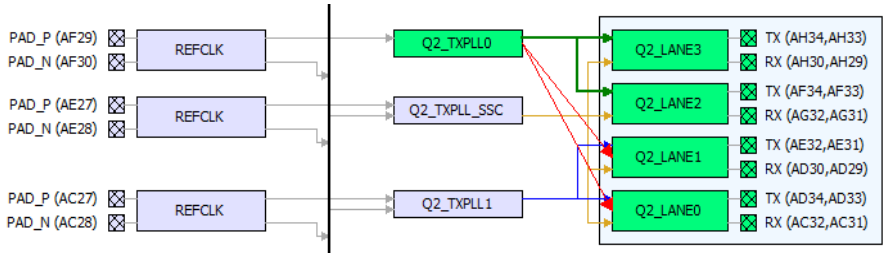


Figure 26 • **Q1_TXPLL1 to Four Lanes Connection (Before Placement)**

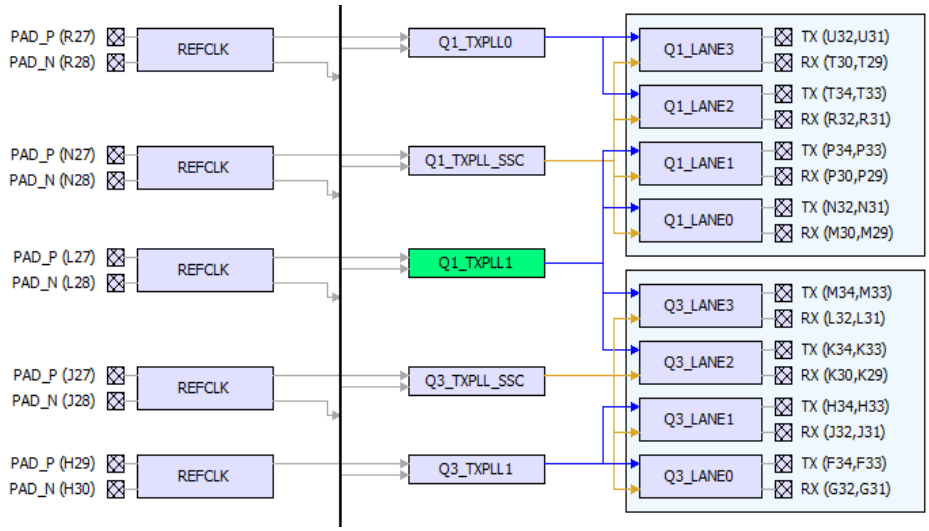
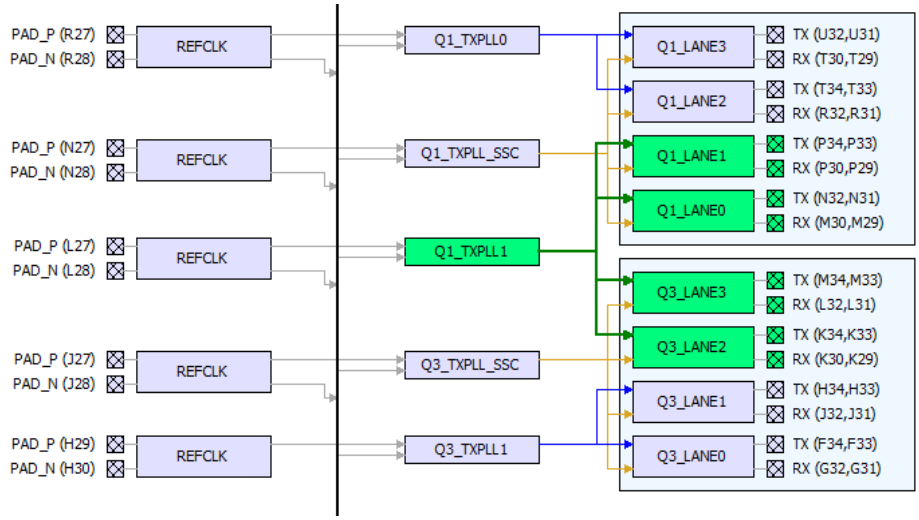


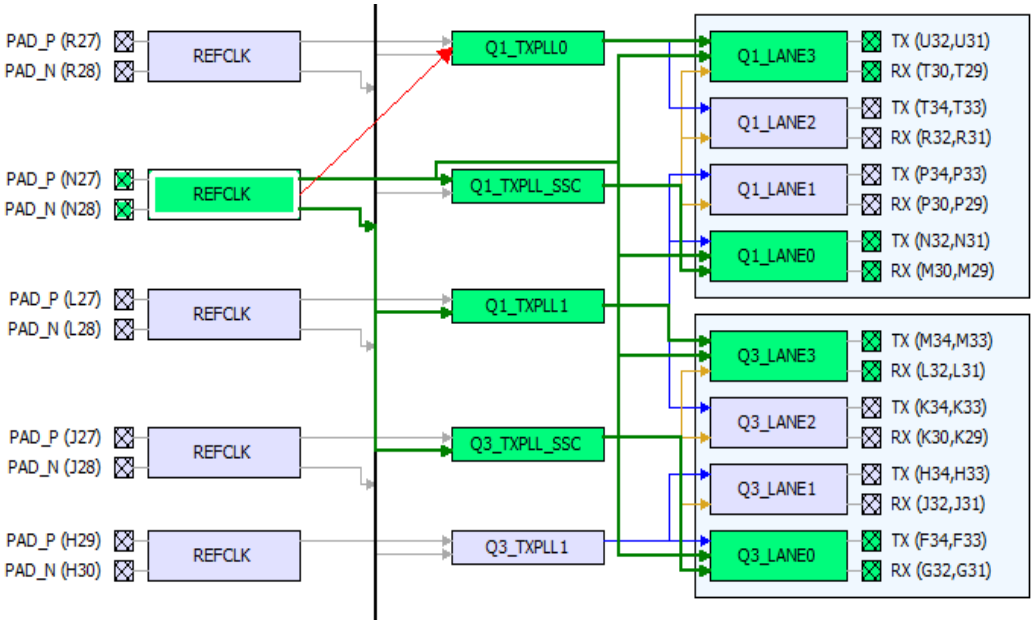
Figure 27 • **Q1_TXPLL1 to Four Lanes Connection (After Placement)**



7.5.2 DRC - REFCLK to TXPLL Connectivity

1. A REFCLK can connect to all the TXPLLs beside and below it (down the Cascade Path) in the Placement View. A REFCLK cannot connect to a TXPLL above it (up the Cascade Path).
2. A cascade path (represented by the vertical line beside the REFCLKs) is used for the REFCLK to connect to all the TXPLLs below it and the Lanes below it in the Placement View.

Figure 28 • **Illegal Connection From REFCLK to TXPLL Up the Cascade Path**

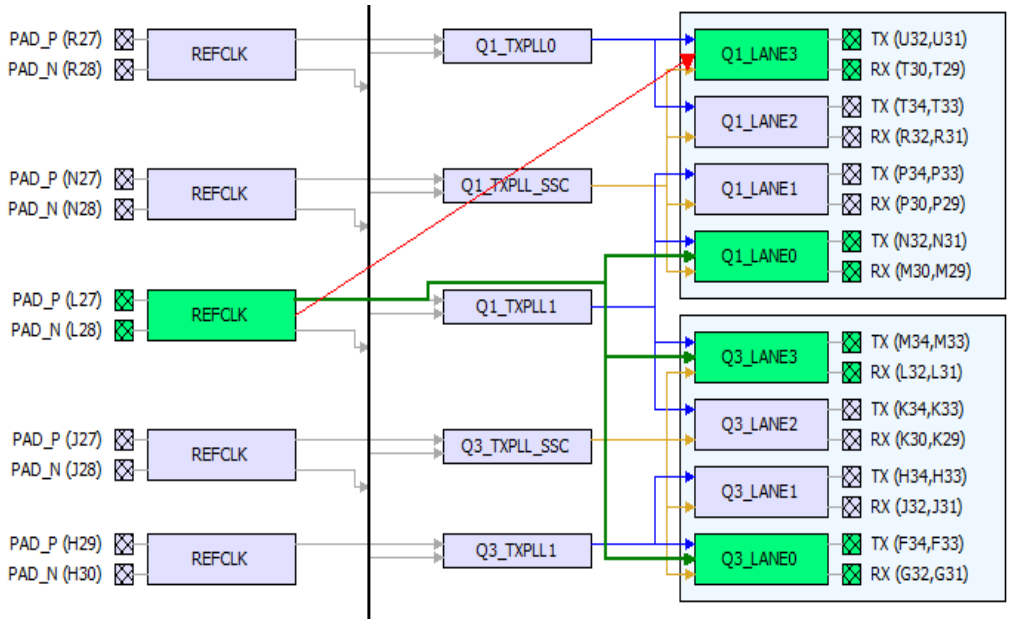


7.5.3 REFCLK To Lanes Connectivity

1. The REFCLK of a quad can connect to all the Lanes the TXPLL beside that REFCLK can connect to, and also all the other Lanes below it (from different quads as well). Connection up the Cascade path is illegal.

Green arrows indicate legal connection and red arrows indicate illegal connection from the REFCLK to the Lanes

Figure 29 • **REFCLK To Lanes Connection - Legal (Down the Cascade Path) and Illegal (Up the Cascade Path)**



8 IOD View

The IOD lane controller handles the complex operations necessary for the high-speed interfaces, such as DDR memory interfaces and CDR interfaces. To bridge the lane clock to the bank clock, the lane controller is used to control an I/O FIFO in each IOD. This I/O FIFO interfaces with DDR memory by utilizing the DQS strobe on the lane clock. The lane controller can also delay the lane clock using a PVT-calculated delay code from the DLL to provide a 90° shift. Certain I/O interfaces require a lane controller to handle the clock-domain that results with higher gear ratios.

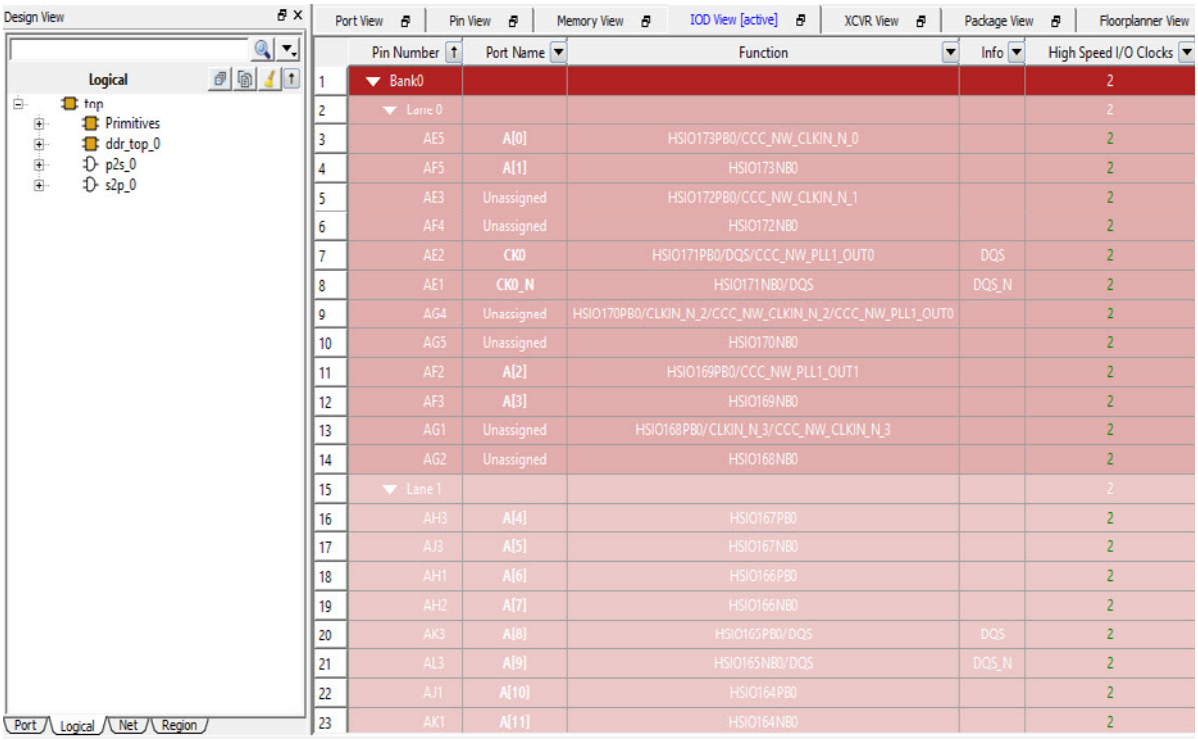
The lane controller also provides the functionality for the IOD CDR. Using the four phases from the CCC PLL, the lane controller creates eight phases and selects the proper phase for the current input condition with the input data. A divided-down version of the recovered clock is provided to the fabric (DIVCLK).

In the PolarFire I/O Editor, the IOD View allows I/O assignments for IOD (I/O Digital) Interface blocks. Libero SoC currently supports CDR and RX_DDR_L_A/TX_DDR_G_A generic IOD interface. Future releases will add in more interfaces. The IOD views presents a hierarchical view of the Generic IOD based on Bank and Lanes. In PolarFire silicon, there may be up to eight banks per chip and six lanes per bank. Bigger dies may have even more lanes per bank.

Notes: The actual number of banks and the number of lanes per bank vary with the die.

When the I/O Editor opens the IOD view, it detects the specific IOD Interface standards, groups the I/Os into specific banks/lanes and populates the spreadsheet-like table with the I/O names (specific to the IOD Interface) accordingly.

Figure 30 • **IOD View**



8.1 Generic I/O Assignments

Drag the I/O port from the Ports tab and drop it to the spreadsheet-like table to make the I/O assignment. The multi-line comment shows the locations where you can legally place the I/O port. Green indicates legal placements, and red indicates illegal placements. Illegal assignments are not allowed.

8.2 DRC Rules

The I/O Editor enforces DRC rules. More DRC rules will be implemented in future releases. The following is a list of the more common DRC rules the I/O Editor enforces.

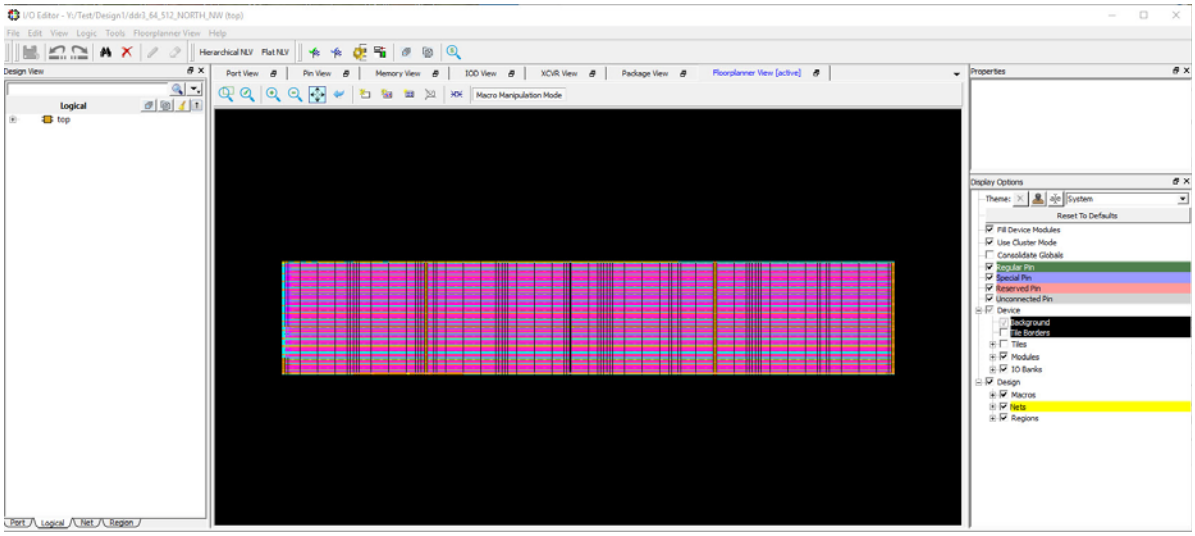
1. All I/Os of the same logical lane must be placed within the same physical lane.
2. For any one physical lane, only one logical lane is allowed to be placed.
3. Non-logical lane I/Os can be placed in any physical lane.
4. For RGMII Interface, the *_RXC port must be placed on the DQS_P side of the physical lane.
5. When the CDR is placed in a physical lane, the DQS_N slot is reserved and is not available to the user for I/O placement.

See UG0686: PolarFire FPGA User I/O User Guide for more DRC rules for IOD I/O placement.

9 Floorplanner View

The Floorplanner View displays all design elements in one window. The selections you make in the views are reflected in the window. The color scheme used in the canvas is dependent on the Layers and Colors you have selected in the Display Options window.

Figure 31 • **Floorplanner View**



9.1 Operation Modes

The Floorplanner View has two modes of operation. Click the **Macro Manipulation Mode** button to switch between Macro Manipulation Mode and Region Manipulation modes:

- **Macro Manipulation Mode**
  Use this mode to work with macros, such as assigning macros to location or unassigning placed macros from locations. You can also view properties of selected macros in the Floorplanner View from the properties window. You can select multiple macros by pressing the <CTRL> key and selecting required macros.
- **Region Manipulation Mode**
  Use this mode to work on regions such as resizing, renaming, or deleting regions, or assigning and unassigning macros or nets to regions.

9.1.1 Display Modes

The Display Options window configures the display of the Floorplanner View. Three display options are available:

- Fill Device Cells
- Use Cluster Mode
- Consolidate Globals

You can also see the colors for different component types (nets, modules, pins, etc.) in the Display Options window.

9.1.2 Floorplanner View Icons

The icons available across the top of the Floorplanner View window allows you to zoom in, zoom out, assign I/O banks, runs DRC checks, create regions for placement.

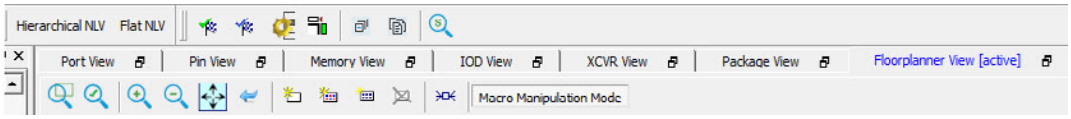


Figure 32 • **Floorplanner View Icons Across the Top of the Window**

Table 10 lists the functions of the each icon.

Table 10 • **Floorplanner View Icons**

Icon	Name	Function
	Rubber Band Zoom	Rubber Band Zoom - Drags out an area to enlarge/zoom into.
	Rubber Band Select	Rubber Band Select an area to Zoom into. Click in the Floorplanner View and drag the mouse to delineate an area. Release the mouse and all macros inside the delineated area are selected. Works in the Macro Manipulation Mode.
	Zoom In	Zoom In to canvas.
	Zoom Out	Zoom Out of canvas.
	Zoom to Fit	Zoom to fit the canvas size.
	Zoom to Location	Zoom to a Location Specified by X-Y co-ordinates.
	Zoom to fit Selection	Zoom to fit selected macros and ports. When enabled, the view attempts to center the view on the selected and placed ports.
	Check Design Rules	Run the Prelayout Checker, a preliminary check of the netlist for possible Place and Route issues.
	Check DRC Rules for Selected Interfaces	Check the DRC Rules for selected interfaces.
	I/O Bank Settings	Set the I/O bank to specific I/O Technology.

Icon	Name	Function
	Auto Assign I/O Bank	Run the Auto I/O Bank and Globals Assigner. Assigns a voltage to every I/O Bank that does not have a voltage assigned to it and if required, a VREF pin.
	Collapse Visible Views	Collapse the visible views.
	Expand Selected Items in Visible Views	Expand selected Items in the visible views.
	Create Empty	Create an empty user region.
	Create Inclusive	Create an inclusive user region.
	Create Exclusive	Create an Exclusive user region.
	Delete	Delete the selected user region.
	Show Nets For Macros	Show all nets connected to the macro. There are often many nets attached to the macro, and it is off by default.

An object or a collection of the objects in the Design View window can be selected and placed in any location that is legal.

Figure 33 shows an example of a successful placement into the Floorplanner View.

Figure 33 • **Floorplanner View—Successful Placement**

9.2 Netlist Views

In addition to the chip view for floorplanning purposes, the Chip Planner displays (in the same Floorplanner View window) a schematic view of the design to make it easier to trace nets and debug the design.

Two netlist types can be displayed in the Floorplanner View window:

- Post-Synthesis Hierarchical View (Hierarchical NLV)
- Post-compile flattened Netlist View (Flat NLV)

The views are identified by tabs across the top of the window after they are loaded into memory. This makes it easy to switch between the different views.

9.2.1 Hierarchical NLV View

The Post-Synthesis Hierarchical View (Hierarchical NLV) is a hierarchical view of the netlist after synthesis and after technology mapping to the Microsemi FPGA technology. Click the **Hierarchical NLV** button to display this view. The Chip Planner loads the netlist into the system memory and displays it in the Floorplanner View window.

When the netlist is loaded for the first time into memory, a pop-up progress bar indicates the progress of the loading process, which may incur some runtime penalty for a large netlist.

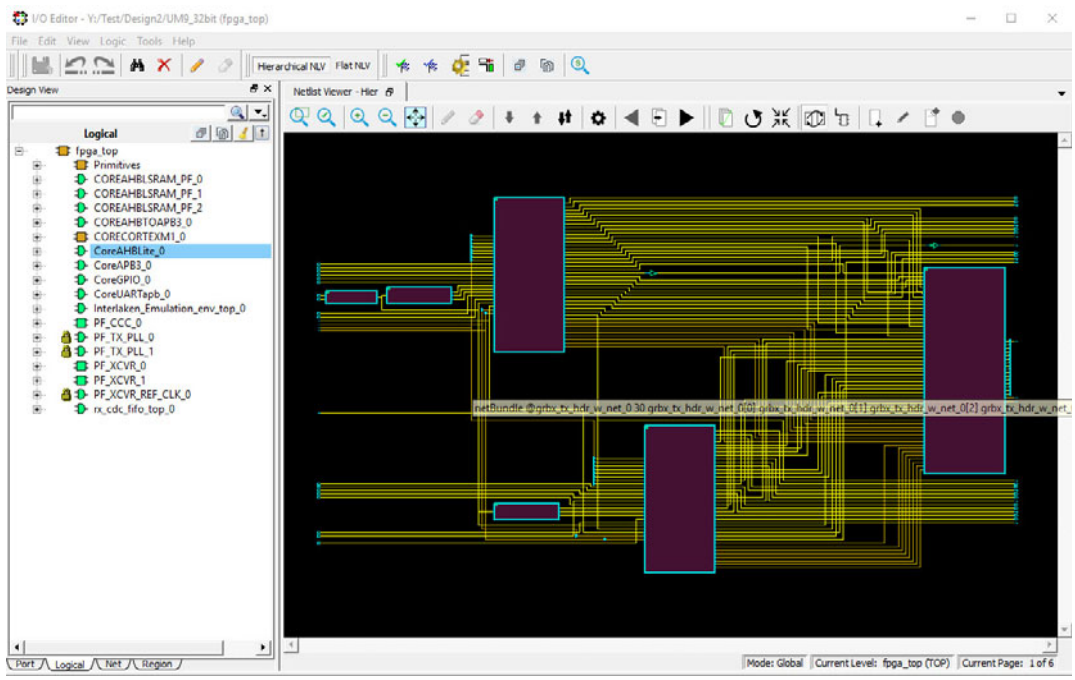


Figure 34 • **Hierarchical NLV View**

9.2.2 Flat NLV View

This is the flattened (non-hierarchical) netlist generated after synthesis, technology mapping and further optimization based on the DRC rules of the device family and/or die. Click the **Flat NLV** button to display this view. The Chip Planner loads the netlist into the system memory and displays it in the Floorplanner View window.

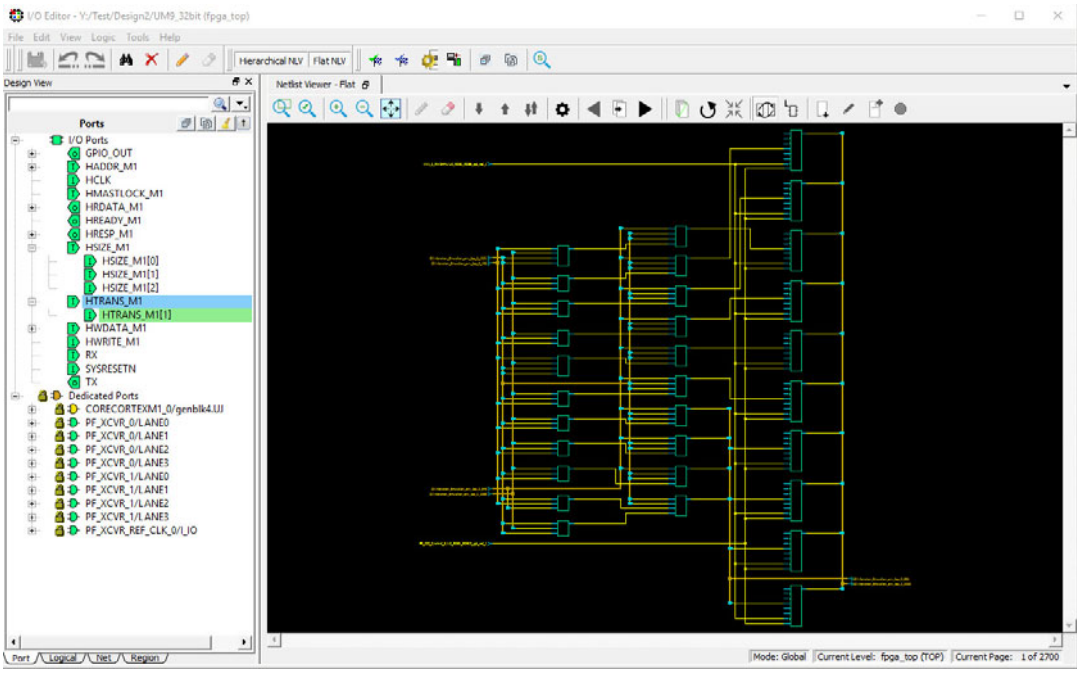


Figure 35 • **Flat NLV View - Flattened Netlist**

9.2.2.1 Display Across Multiple Pages

Hierarchical or flattened netlists can span multiple pages, in which case the first page is displayed when it opens.

The current page number and the total number of pages are displayed in the status bar at the lower right corner of the window.

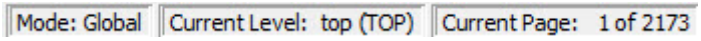


Figure 36 • **Status Bar**

To go to different pages of the Netlist view, use the left-pointing arrow  or right-pointing arrow  .

9.2.3 Netlist Viewer Features

See the Netlist Viewer Interface User Guide for details about Netlist Viewer features.

9.2.4 Chip Planner Features

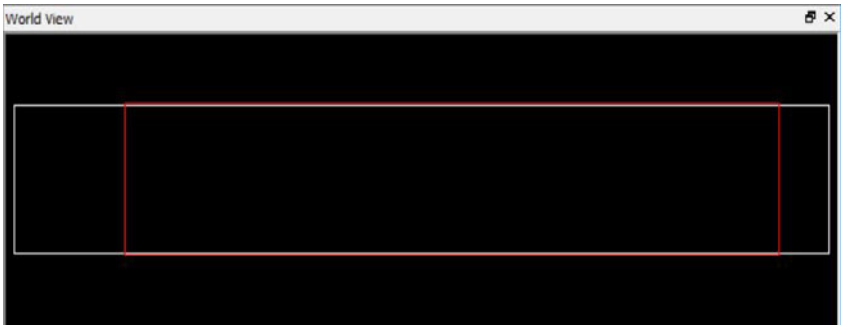
See the Chip Planner User Guide for details about Chip Planner features.

10 Other I/O Editor Windows

10.1 World View Window

The World View shows a red rectangle which reflects what is visible in the Floorplanner View in the context of the die. Changing what is visible in the canvas also changes the red rectangle. Changing the size or position of the red rectangle changes what is seen in the Floorplanner View.

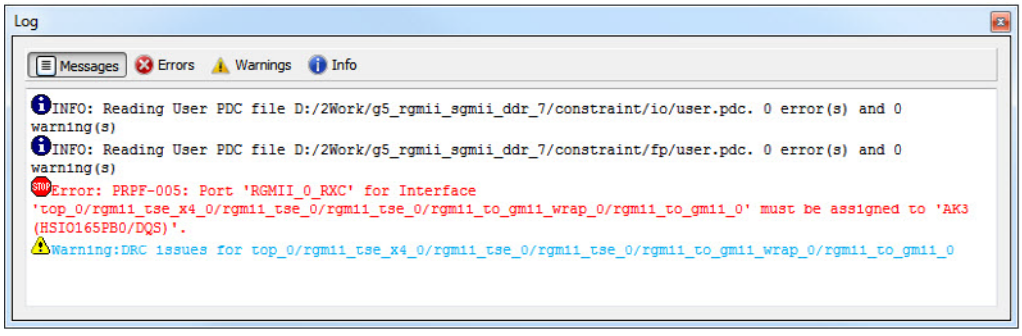
Figure 37 • **World View Window**



10.2 Log Window

The Log window displays all messages generated by I/O Editor. You can filter the messages according to the type of message: Error, Warning, and Info. If you have made and saved changes in I/O Editor, the Log window displays the name and location of the PDC file(s) which have been edited/updated to reflect the changes.

Figure 38 • **Log Window**



10.3 Display Options Window

The Display Options window configures the display of the selected viiew. Three display options are available:

- Fill Device Cells
- Use Cluster Mode
- Consolidate Globals

10.4 Properties Window

The Properties window displays the properties of the design elements. What is displayed in the Properties window is dependent on what is selected in the design view. Properties displayed may include the following, depending on the type of design elements:

- Macro/Component Name - Full Macro or component name based on selection.
- Cell Type - Resource type based on design element selection.
- Placed (Location) - X-Y coordinates where device element is placed.
- Resource Usage Table - A table showing resources based on component and macro selection.
- Region Attached Table - A table showing region to which selected macro/component is assigned.
- User region (if any) it is attached to.
- Nets Table - A table showing pins and nets which is associated with the selected macro along with
  fanout value.
- Locked/Unlocked (Placement) - The selected port is locked or unlocked.
- Port - Port name to which the I/O macro is assigned (only shown for I/O port macros).
- I/O Technology Standard - I/O Technology which is associated with the selected I/O macro (only
  shown for I/O port macros).
- I/O Bank- I/O bank to which the selected I/O macro is assigned (only shown for I/O port macros).
- Pin (Package Pin) - Pin to which the macro is assigned (only shown for I/O port macros).

Not all properties in the list are displayed. The list of displayed properties varies with the type of design element selected.

11 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

11.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

11.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

11.3 Technical Support

For Microsemi SoC Products Support, visit
http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

11.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

11.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

11.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

11.5.2 My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

11.5.3 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

11.6 ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.