PolarFire® SoC FPGA Devices Errata

Introduction

The PolarFire® SoC FPGA family devices are subjected to the limitations described in this errata document. This document contains updated information about known devices specific issues and provides the available limitations and workarounds. Contact Microchip Technical Support for more information.

PCB Designs

For information about how to determine proper signal pinout, see PolarFire SoC FPGA Board Design Guidelines User Guide. The proper signal pinout is needed for all clocking, transceiver, and FPGA pin recommendations.

Device Identification

PolarFire SoC FPGA production samples can be identified as shown in the following figures.

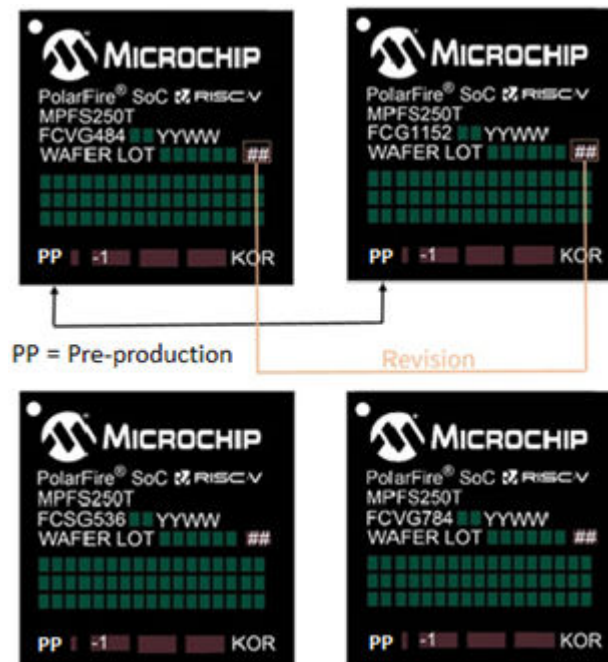**Figure 1. Device Identification Markings: Pre-Production Devices**

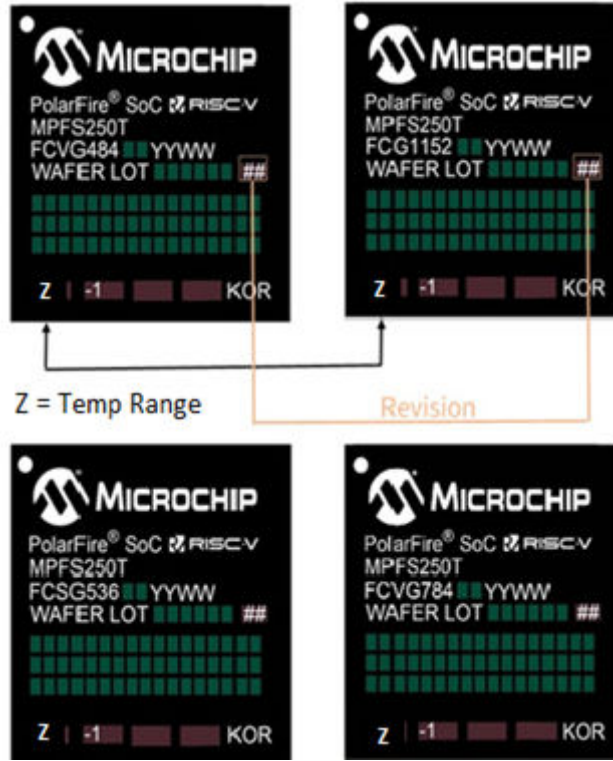**Figure 2. Device Identification Markings: Production Devices**

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1. Errata Descriptions and Workarounds

The following section describes the device errata and the workarounds. The following table lists the errata for Engineering Samples (ES), Pre-Production (PP) silicon, and production silicon. For device part marking specifications, see 2. Device Identification.

Table 1-1. Summary of PolarFire® SoC FPGA Errata

PolarFire® SoC MPFS250T Errata History	Silicon Revisions			
Description	**ES[1]**	**Pre-Production**		**Production**
	Revision 0	**Revision 0**	**Revision 1**	**Revision 0**
Microprocessor Subsystem (MSS) cannot access system controller SPI flash	*	X	X	X
AXI Switch Memory Protection Unit (MPU) is not operational	*	X	X	X
MSS I^{2}C peripheral works only with MSS core version 2.0.108 and above	*	X	X	X
When MSS CPU's frequency is limited to 600 MHz	*	X	X	X
When MSS works as a master, DRI interrupt line must not be used	*	X	X	X
DRI error and DRI fault interrupts are not connected to the maintenance interrupt	*	X	X	X
MSS GPIO configuration registers must only be reset by the CPUs	*	X	X	X
Fabric APB DRI's slow writes corrupt the SmartDebug JTAG/SPI read data	*	X	X	X
System controller suspend mode is not supported	*	X	X	X

..........continued				
PolarFire® SoC MPFS250T Errata History	**Silicon Revisions**			
Description	**ES[1]**	**Pre-Production**		**Production**
	Revision 0	**Revision 0**	**Revision 1**	**Revision 0**
PolarFire SoC MSS GEM (Gigabit Ethernet MAC) has an issue with Undersize Frame Counter in Ethernet statistics	*	X	X	X
Auto-program or Auto-update of eNVM should not be used	*	X	X	X
Auto-update system service allows SPI master mode to be used incorrectly configured for SPI slave mode	*	X	X	X
JTAG zeroization at the end of programming causing auto programming to kick in post zeroizing	*	*	X	X

Notes:

1. Refers to Errata for PolarFire SoC ES devices.
2. '*'—Indicates that that the errata exists for the specified silicon revision.
3. 'X'—Indicates that the issue is fixed in the specified silicon revision.

1.1 Production Validation Status

This section details the PolarFire SoC MPFS025T and PolarFire SoC MPFS250T product validation status for Revision 0.

1.1.1 eMMC HS400 and HS400 Enhanced Strobe Modes

eMMC validation over process, voltage, and temperature is completed for all the supported modes except for eMMC HS400 and HS400 Enhanced Strobe (HS400-ES) modes. The validation status is listed as follows:

- HS400 mode: Compliance is in progress.
- HS400-ES mode: Validation and compliance are in progress.

See *PolarFire SOC MSS Technical Reference Manual* for more information about eMMC supported modes or contact Microchip Technical Support.

1.1.2 LPDDR4 Bring Up, Debug, and Validation

LPDDR4 validation over process, voltage, and temperature is completed. See PolarFire® SoC FPGA Board Design Guidelines User Guide for reference board design files and board design practices to achieve expected performance from PCBs and PolarFire SoC devices.

> **Important:** Additional collateral is created to provide guidelines for design, bring up, debug, and validation of LPDDR4-based system. This collateral will be available by July 2022. Contact Microchip Technical Support for more information.

1.1.3 SD Compliance

The following lists the SD compliance status.

- SD validation over process, voltage, and temperature is completed for all the modes.
- Compliance is completed for SD-DS and SD-HS modes.
- Compliance for UHS-I SDR12, UHS-I SDR25, UHS-I SDR50, UHS-I SDR104, and UHS-I DDR50 is in progress.

See *PolarFire SOC MSS Technical Reference Manual* for more information about SD supported modes or contact Microchip Technical Support.

2. Libero® SoC Software Errata

For Libero SoC related issues and limitations, see Libero SoC Release Notes.

3. Embedded Software Errata

See SoftConsole Release Notes for more information.

4. Revision History

Revision	Date	Description
B	06/2022	Made changes to the revision history and releasing this document for Production Device.
A	06/2022	Internal Release

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