Technical Note

Calculating Memory Power for DDR4 SDRAM

Introduction

DDR4 SDRAM provides additional bandwidth over previous DDR3 SDRAM. In addition to the increased performance, DDR4 has a lower operating voltage range. DDR4 also added a word-line boost supply of 2.5V to provided more efficient power delivery than pumping all the way from 1.2V. The result can be a system performing at higher bandwidth while consuming equal or less system power. However, it is not always easy to determine the power consumption within a system application from the data sheet specification.

This technical note details how DDR4 SDRAM consumes power and provides the tools that system designers can use to estimate power consumption in any specific system. In addition to offering tools and techniques for calculating system power, Micron's DDR4-2666 "Data Sheet Specifications" and a DDR4 Power Spreadsheet Usage Example are provided.

Table 1 describes the command abbreviations found in the following sections.

Table 1: Abbreviation Definitions

Abbreviation	Definition
ACT	ACTIVATE
BL	Burst length
BC	Burst chop
PRE	PRECHARGE
ODT	On-die termination
RD	READ
REF	REFRESH
WR	WRITE

DRAM Operation

To estimate the power consumption of DDR4 SDRAM, it is necessary to understand the basic functionality of the device (see the following figure). The operation of a DDR4 device is similar to that of a DDR3 SDRAM. For both devices, the master operation of the DRAM is controlled by clock enable (CKE).

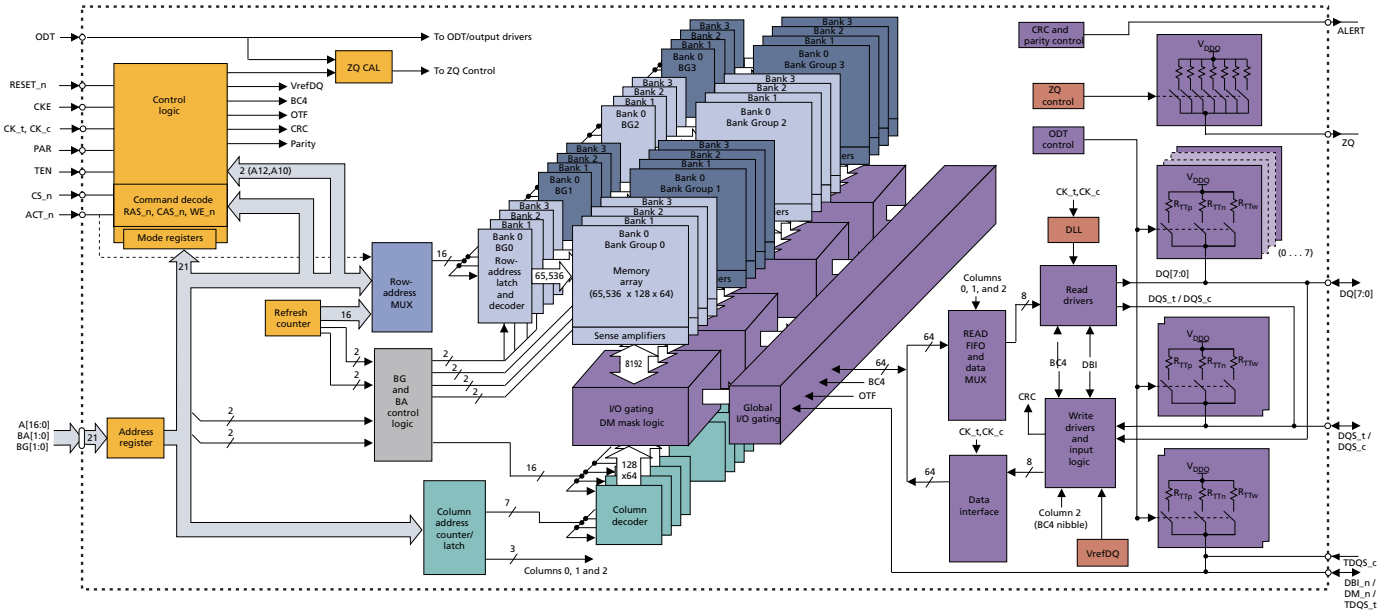
If CKE is LOW, the input buffers are turned off. For the DRAM to receive commands, CKE must be HIGH, enabling the input buffers and propagating the command/address into the logic/decoders on the DRAM.

During normal operation, the first command sent to the DRAM is typically an ACT command. This command selects a bank and row address. The data, which is stored in the cells of the selected row, is then transferred from the array into the sense amplifiers. The portion of the DRAM consuming power in the ACT command is shown in blue and gold in the figure below.

Sixteen different array banks, four per each bank group, exist on the x4 and x8 DDR4 SDRAM. The x16 device has only eight different array banks from two bank groups. Each bank contains its own set of sense amplifiers and can be activated separately with a unique row address. When one or more banks has data stored in the sense amplifiers, the DRAM is in the active state.

The data remains in the sense amplifiers until a PRE command to the same bank restores the data to the cells in the array. Every ACT command must have a PRE command associated with it; that is, ACT and PRE commands occur in pairs unless a PRECHARGE ALL command is used.

Figure 1: 8Gb, x8 DDR4 SDRAM Functional Block Diagram



In the active state, the DDR4 device can perform READs and WRITEs. A READ command decodes a specific column address associated with the data that is stored in the sense amplifiers (shown in green in the above figure). The data from this column is driven through the I/O, gating to the internal READ latch. From there, it is multiplexed onto

the output drivers. The circuits used in this function are shown in purple in the above figure.

The process for a WRITE is similar to the READ except that the data propagates in the opposite direction. Data from the DQ pins is latched into the data receivers/registers and is transferred to the internal data drivers. The internal data drivers then transmit the data to the sense amplifiers through the I/O gating and into the decoded column address location.

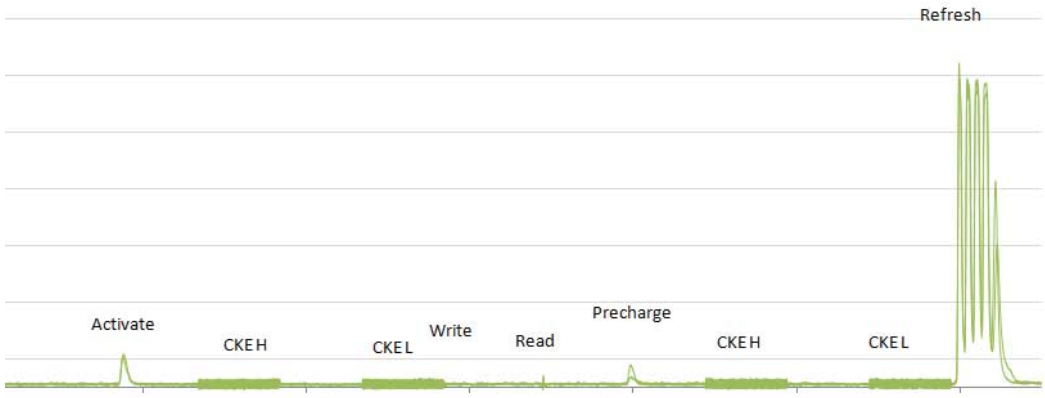
DDR4 technology, like DDR3, includes ODT on the data I/O pins. This feature is controlled by the ODT pin and consumes additional power when activated. The ODT and the output driver on DDR4 devices include additional mode register settings over previous DRAM to increase system flexibility and to optimize signal integrity. This power needs to be included in total power calculations (see "I/O Termination Power" on page 13).

As noted, DDR4 technology added a V_{PP} supply for the DRAM internal word line boost. A key difference between the DDR4 Power Calculator and the DDR3 Power Calculator is the DDR4 Power Calculator (both available on micron.com) includes V_{PP} power coverage. The majority of V_{PP} current occurs during an ACT, PRE or REF command as one might expect; a picture of typical, real time I_{PP} current draw is shown in the figure below.

The DDR4 device calculation procedure annotates the V_{PP} supply needs where applicable and mirrors the V_{DD} analysis.

- For the standby currents, there is an IPP2P when I_{DD2P} is applicable, an I_{PP2N} when I_{DD2N} is applicable, an I_{PP3P} when I_{DD3P} is applicable, and an I_{PP3N} when I_{DD3N} is applicable. I_{PP3N} (some times referred to as I_{PPSB}) is used in place of I_{PP2P}, I_{PP2N} and I_{PP3P} because they are very similar.
- For read and write currents, there is an I_{PP4R} and an I_{PP4W} when I_{DD4R} is applicable. I_{PP4R} and I_{PP4W} also use I_{PP3N} because they are equal to or slightly less than I_{PP3N}.
- For the activate and refresh currents, there is an I_{PP0} when I_{DD0} is applicable and an I_{PP5B} when I_{DD5B} is applicable.

Figure 2: V_{PP} Currents Command Dependant



DRAM Power Calculators

The I_{DD} values referenced in this article are taken from Micron's 8Gb DDR4-2666 data sheet and are listed in the Data Sheet Specifications section. While the values provided in data sheets may differ from between vendors and different devices, the concepts for calculating power are the same. It is important to verify all data sheet parameters before using the information in this article.

Methodology Overview

The following four steps are required to calculate system power:

1. Calculate the power subcomponents from the data sheet specifications. (This calculation is denoted as Pds(XXX), where XXX is the subcomponent power.)
2. Derate the power based on the command scheduling in the system (Psch[XXX]).
3. Derate the power to the system's actual operating V_{DD} and clock frequency (Psys[XXX]).
4. Find the sum of the subcomponents of the system's operating conditions to calculate the total power consumed by the DRAM.

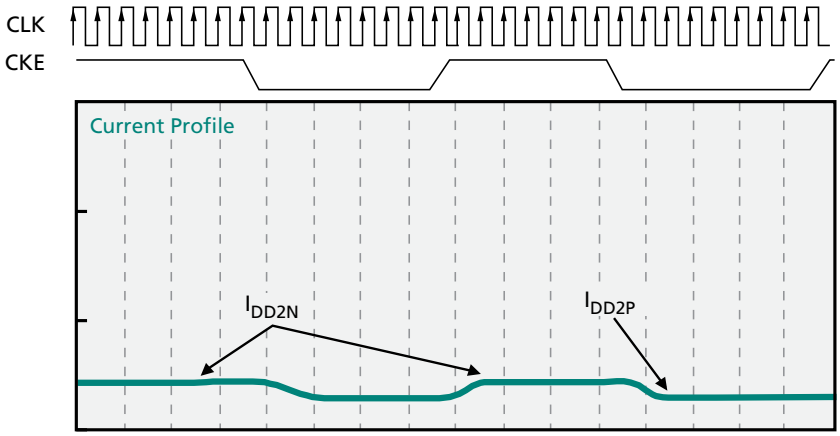
Background Power

As discussed previously, CKE is the master on/off switch for DDR4 SDRAM. When CKE is LOW, most inputs are disabled. This is the lowest power state in which the device can operate, and if all banks are precharged, it is specified in the data sheet as I_{DD2P}. If any bank is open, the current consumed is I_{DD3P}.

CKE must be taken HIGH to allow the DRAM to receive ACT, PRE, READ and WRITE commands. When CKE goes HIGH, commands start propagating through the DRAM command decoders, and the activity increases the power consumption. The current consumed is specified in the data sheet as I_{DD2N} if all banks are precharged or I_{DD3N} if any bank is active.

The follwing figure shows the typical current usage of a DDR4 device when CKE transitions, assuming all banks are precharged. When CKE is HIGH, the device draws a maximum I_{DD2N} current of 35mA; when CKE goes LOW, that figures drops to an I_{DD2P} of 25mA. Both of these values assume the DRAM is in the precharged state. Similarly, if the device is in the active state, it consumes I_{DD3P} current in power-down (CKE = LOW) and I_{DD3N} current in standby (CKE = HIGH).

Figure 3: Effects of CKE on I_{DD} Consumption



Calculation of the power consumed by a DDR4 device operating in these standby conditions is easily completed by multiplying the I_{DD} and the voltage applied to the device, V_{DD}.

Table 2: Standby Power Formulas – V_{DD} Supply

Formula	Equation
Pds(PRE_PDN) = $I_{DD2P} \times V_{DD}$	1
Pds(PRE_STBY) = $I_{DD2N} \times V_{DD}$	2
Pds(ACT_PDN) = $I_{DD3P} \times V_{DD}$	3
Pds(ACT_STBY) = $I_{DD3N} \times V_{DD}$	4

Table 3: Standby Power Formulas – V_{PP} Supply

Formula	Equation
Pdsp(PRE_PDN) = $_{IPP2P} \times V_{PP}$ --> $I_{PP3N} \times V_{PP}$	1a
Pdsp(PRE_STBY) = $I_{PP2N} \times V_{PP}$ --> $I_{PP3N} \times V_{PP}$	2a
Pdsp(ACT_PDN) = $I_{PP3P} \times V_{PP}$ --> $I_{PP3N} \times V_{PP}$	3a
Pdsp(ACT_STBY) = $I_{PP3N} \times V_{PP}$	4a

The data sheet specification for all I_{DD} and I_{PP} values is taken at the worst-case V_{DD}, which is 1.260V and worst-case V_{PP}, which is 2.75V for DDR4. The calculations for maximum DDR4 standby powers using the assumptions in the Data Sheet Specifications section are as shown in the following tables.

Table 4: Standby Power Calculations – V_{DD} Supply

Formula	Equation
Pds(PRE_PDN) = 25mA × 1.26V Pds(PRE_PDN) = 31.5mW	5
Pds(PRE_STBY) = 35mA × 1.26V Pds(PRE_STBY) = 44.1W	6

Table 4: Standby Power Calculations – V_{DD} Supply (Continued)

Formula	Equation
Pds(ACT_PDN) = 39mA × 1.26V Pds(ACT_PDN) = 49.1mW	7
Pds(ACT_STBY) = 46mA × 1.26V Pds(ACT_STBY) = 58mW	8

Table 5: Standby Power Calculations – V_{PP} Supply

Formula	Equation
Pdsp(PRE_PDN) = 3mA × 2.75V Pdsp(PRE_PDN) = 8.3mW	5a
Pdsp(PRE_STBY) = 3mA × 2.75V Pdsp(PRE_STBY) = 8.3mW	6a
Pdsp(ACT_PDN) = 3mA × 2.75V Pdsp(ACT_PDN) = 8.3mW	7a
Pdsp(ACT_STBY) = 3mA × 2.75V Pdsp(ACT_STBY) = 8.3mW	8a

During normal operation, the DRAM always consumes background power. This background power can be in one of the four categories above. Therefore, the total average background power is a ratio of these four individual powers. This ratio is determined by the percentage of time the DRAM is precharged (all of the banks are precharged) or active (one or more banks are open). Additionally, the percent of time that CKE is LOW or HIGH during each of the conditions determines the ratio between the standby and the power-down conditions. The three parameters required to complete these ratios are shown in the following table.

Table 6: DDR4 Background Power Components

Component	Description
BNK_PRE%	Percentage of time all banks are precharged
CKE_LO_PRE%	Percentage bank precharge time (BNK_PRE%) when CKE is LOW
CKE_LO_ACT%	Percentage bank active time (100% - BNK_PRE%) when CKE is LOW

Equation 9 is used to determine the ratio of the data sheet background powers to the specific system usage conditions based on CKE HIGH/LOW times. Note that these numbers cover 100% of the normal device operating time.

Table 7: Standby Power With CKE Control – V_{DD} Supply

Formula	Equation
Psch(PRE_PDN) = Pds(PRE_PDN) × BNK_PRE% × CKE_LO_PRE%	9
Psch(PRE_STBY) = Pds(PRE_STBY) × BNK_PRE% × [1-CKE_LO_PRE%]	
Psch(ACT_PDN) = Pds(ACT_PDN) × [1-BNK_PRE%] × CKE_LO_PRE%	
Psch(ACT_STBY) = Pds(ACT_STBY) × [1-BNK_PRE%] × [1-CKE_LO_PRE%]	

Table 8: Standby Power With CKE Control – V_{PP} Supply

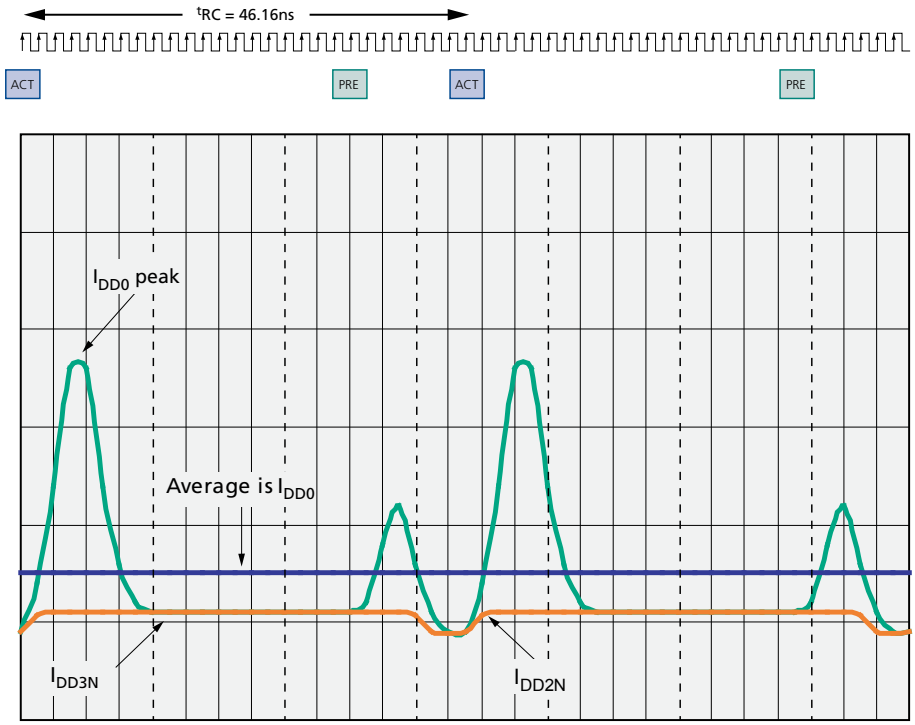
Formula	Equation
Pschp(PRE_PDN) = Pdsp(PRE_PDN) × BNK_PRE% × CKE_LO_PRE%	9a
Pschp(PRE_STBY) = Pdsp(PRE_STBY) × BNK_PRE% × [1-CKE_LO_PRE%]	
Pschp(ACT_PDN) = Pdsp(ACT_PDN) × [1-BNK_PRE%] × CKE_LO_PRE%	
Pschp(ACT_STBY) = Pdsp(ACT_STBY) × [1-BNK_PRE%] × [1-CKE_LO_PRE%]	

Activate Power

To enable a DDR4 SDRAM to READ or WRITE data, a bank and row must first be selected using an ACT command. For every ACT command, there is a corresponding PRE command. The ACT command opens a row, and the PRE closes the row.

The following figure illustrates a typical current profile for I_{DD0}. Following an ACT command, the device uses a significant amount of current to decode the command/address and then transfer the data from the DRAM array to the sense amplifiers. When this is complete, the DRAM is maintained in an active state until a PRE command is issued. The PRE command restores the data from the sense amplifiers into the memory array and resets the bank for the next ACT command. This leaves the bank in its precharged state.

Figure 4: I_{DD0} Current Profile



Note: 1. Current profiles are provided for illustrative purposes and are not associated with a specific DDR4 DRAM device.

The data sheet specifies I_{DD0} averaged over time with the interval between ACT commands being ^{t}RC. This is represented by the blue line in the figure above. During this operation, a background current, shown in orange, is always consumed (I_{DD3N} when the row is active and I_{DD2N} when the row is precharged). This background current must be subtracted from I_{DD0} to identify the power consumed due to the ACT and PRE commands. This is shown in Equation 10, where I_{DD3N} is subtracted from I_{DD0} during the row active time (^{t}RAS) and I_{DD2N} is subtracted during the remaining time.

Table 9: Active Power – V_{DD} Supply

Formula	Equation
$Pds(ACT) = (I_{DD0} - [I_{DD3N} \times {}^{t}RAS / {}^{t}RC + I_{DD2N} \times ({}^{t}RC - {}^{t}RAS) / {}^{t}RC]) \times V_{DD}$ $Pds(ACT) = (51mA - [46mA \times 32ns / 46.16ns + 35mA \times (46.16ns - 32ns) / 46.16ns]) \times 1.26V$ **Pds(ACT) = 10.6mW**	10

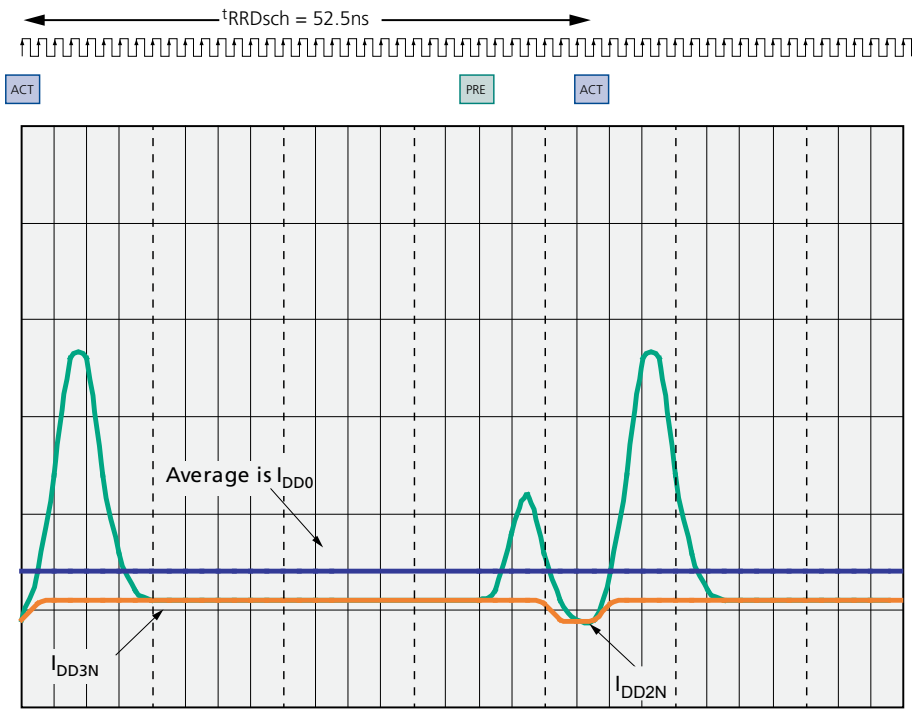
Table 10: Active Power – V_{PP} Supply

Formula	Equation
$Pdsp(ACT) = (I_{PP0} - [I_{PP3N} \times {}^{t}RAS / {}^{t}RC + I_{PP2N} \times ({}^{t}RC - {}^{t}RAS) / {}^{t}RC]) \times V_{PP}$ $Pdsp(ACT) = (3mA - [2.4mA \times 32ns / 46.16ns + 2.4mA \times (46.16ns - 32ns) / 46.16ns]) \times 2.75V$ **Pdsp(ACT) = 1.7mW**	10a

Note: 1. Because I_{PP0}, I_{PP3N} and I_{PP2N} have the same specification limits, I_{PP3N} and I_{PP2N} are reduced by 20% for estimating actual use differences.

Equation 10 provides the maximum power consumed only if the DRAM is used at MIN ^{t}RC cycle time as specified in the data sheet. This is noted as Pds(ACT), meaning "power under data sheet conditions." However, most systems do not operate in this manner. Fortunately, it is easy to scale the ACT power for other modes of operation. The scaling factor is represented as $^{t}RRDscheduled$ ($^{t}RRDsch$), which is the average scheduled row-to-row activate timing. Two examples of scaling activate power with different command spacings are shown. One example is when $^{t}RRDsch > {}^{t}RC$ and a second when the device is in bank interleave mode when $^{t}RRDsch < {}^{t}RC$.

Figure 5: ACT-ACT Current with tRRDsch = 52.5ns



In the above figure, the average ACT-ACT cycle time is greater than the specified tRC = 46.16ns. tRRDsch is stretched to 70 clock cycles, which is 52.5ns for a 1333 MHz clock.

The active power can easily be scaled as the ratio of the actual tRRDsch value to the data sheet tRC condition. The calculation is shown in the following tables.

Table 11: Long tRRD Factor On Active Power – V_{DD} Supply

Formula	Equation
Psch(ACT) = Pds(ACT) × tRC / tRRDsch Psch(ACT) = 10.6mW × 46.16ns / 52.5ns **Pds(ACT) = 9.3mW**	11

Table 12: Long tRRD Factor On Active Power – V_{PP} Supply

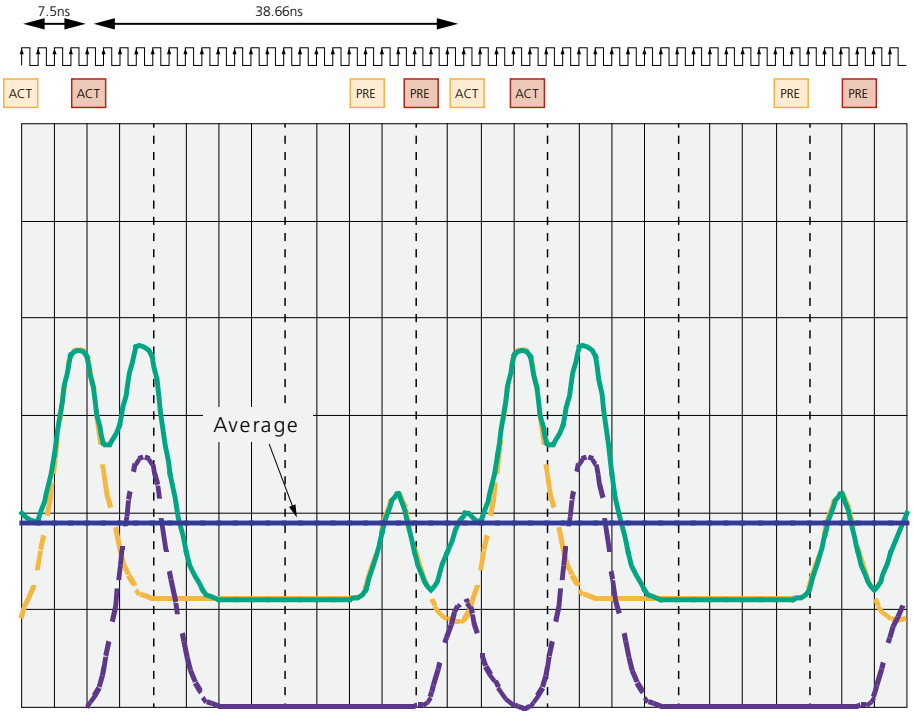
Formula	Equation
Pschp(ACT) = Pdsp(ACT) × tRC / tRRDsch Pschp(ACT) = 1.7mW × 46.16ns / 52.5ns **Pdsp(ACT) = 1.5mW**	11a

Therefore, by changing the ACT-ACT time from 46.16ns to 52.5ns, the maximum activation power, Psch(ACT), drops from 10.6mW to 9.3mW. Note that this power is only the activation power and does not include the background power contributed by I_{DD2N} and I_{DD3N}.

Because a DDR4 device has multiple banks, it is possible to have several open rows at one time. Therefore, it is also possible to have ACT commands closer together than tRC.

the following figure shows an example in which two banks are interleaved within 46.16ns, making the average ^{t}RRDsch = 23.08ns. Because ^{t}RRDsch is an average, it does not matter that some commands are spaced 7.5ns apart while others are 38.66ns apart (see the following figure). The yellow current profile represents the first bank activated and includes the I_{DD3N} component. This is only included in one instance on the device, even if other banks are open. The purple current profile, which represents the second bank activated, shows only the additional current introduced due to the second bank activated. The green curve represents the sum of the two banks.

Figure 6: ACT-ACT Current with ^{t}RRDsch = 23.08ns



The calculation to determine the power consumption for the activation power, shown in the following tables, is the same as before.

Table 13: Short ^{t}RRD Factor On Active Power – V_{DD} Supply

Formula	Equation
Psch(ACT) = Pds(ACT) × ^{t}RC / ^{t}RRDsch Psch(ACT) = 10.6mW × 46.16ns / 23.08ns **Pds(ACT) = 21.2mW**	12

Table 14: Short ^{t}RRD Factor On Active Power – V_{PP} Supply

Formula	Equation
Pschp(ACT) = Pdsp(ACT) × ^{t}RC / ^{t}RRDsch Pschp(ACT) = 1.7mW × 46.16ns / 23.08ns **Pdsp(ACT) = 3.4mW**	12a

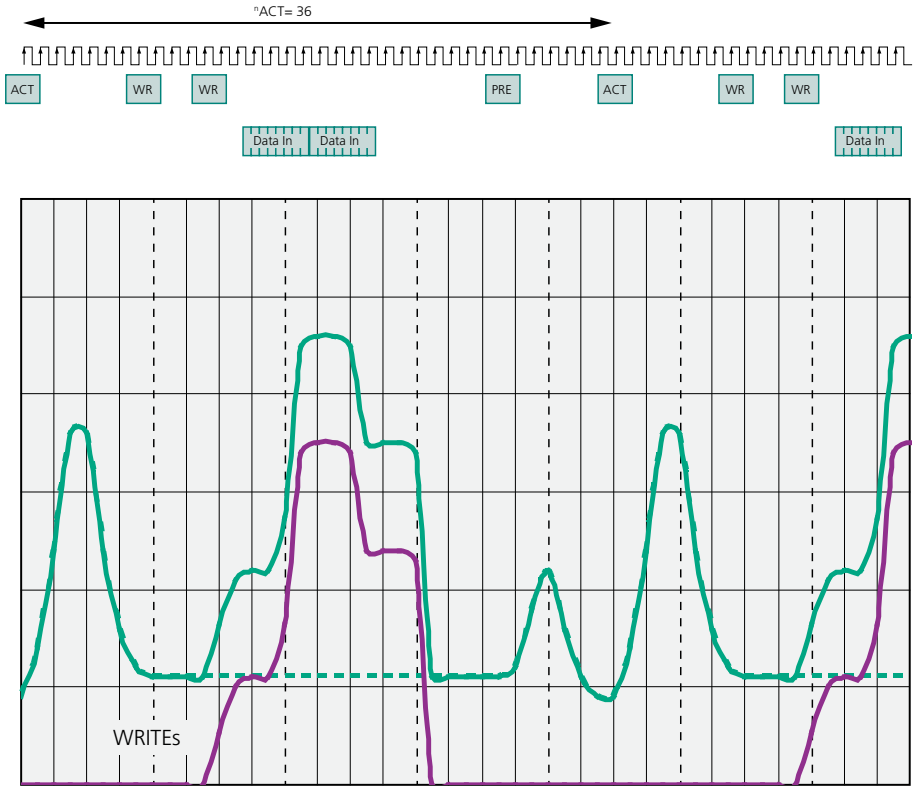
The maximum Psch(ACT) for two interleaved banks increases from 10.6mW to 21.2mW because twice the amount of ACT and PRE power is consumed when operating two banks compared to one.

With this basic equation, ACT-PRE power can be calculated for any usage condition, from sixteen interleaved banks to one bank that is seldom opened.

Write Power

After a bank is open, data can be either read from or written to the DDR4 SDRAM. The two cases are similar. The figure below illustrates an example of two WRITE commands utilizing BL = 8 operation.

Figure 7: Current Profile – WRITEs



When several WRITEs are added between ACT commands, the consumption of current associated with the WRITE is IDD4W. To identify the power associated with only the WRITEs and not the standby current, IDD3N must be subtracted. The calculation for the data sheet write component of power, Pds(WR), is shown in Equation 13.

Table 15: Base Write Power – V_{DD} Supply

Formula	Equation
Pds(WR) = (I_{DD4W} - I_{DD3N}) × V_{DD} Pds(WR) = (132mA - 46mA) × 1.26V **Pds(WR) = 108.4mW**	13

Table 16: Base Write Power – V_{PP} Supply

Formula	Equation
Pdsp(WR) = (I_{PP4W} - I_{PP3N}) × V_{PP} Pdsp(WR) = (3mA - 3mA) × 2.75V **Pdsp(WR) = 0mW**	13a

To scale the data sheet power to actual power based on command scheduling, it must be calculated as a ratio of the write bandwidth. This is noted as WRsch%, which is the total number of clock cycles that write data is on the bus (not WRITE commands) versus the total number of clock cycles. The WRsch% calculation for the example show in the previous figure is shown in Equation 14.

Table 17: Scaling Write Power – V_{DD} and V_{PP} Supply

Formula	Equation
WRsch% = Num_of_writes_cycle / *n*ACT WRsch% = 8 cycles / 36*n*CK **WRsch% = 22%**	14

When the ratio of WRITEs is known, the power associated with the scheduled WRITEs, Psch(WR), can be easily calculated from the data sheet write power, as shown in Equation 15.

The data sheet conditions specify I_{DD4W} with a BL = 8. DDR4 devices may also operate with BC = 4. However, internally the DDR4 SDRAM continues operate as if it were doing BL = 8 WRITEs and masks off the last four data bits. Therefore, if a WRITE using BC = 4 is completed, it will require approximately the same amount of power as a WRITE with BL = 8 (four clock cycles). The multiplication of the (8/BL) at the end of the equation adjusts for this difference in burst length.

Table 18: Scaled Write Power – V_{DD} Supply

Formula	Equation
Psch(WR) = Pds(WR) × WRsch% Psch(WR) = 108.4mW × 22% **Psch(WR) = 23.8mW**	15

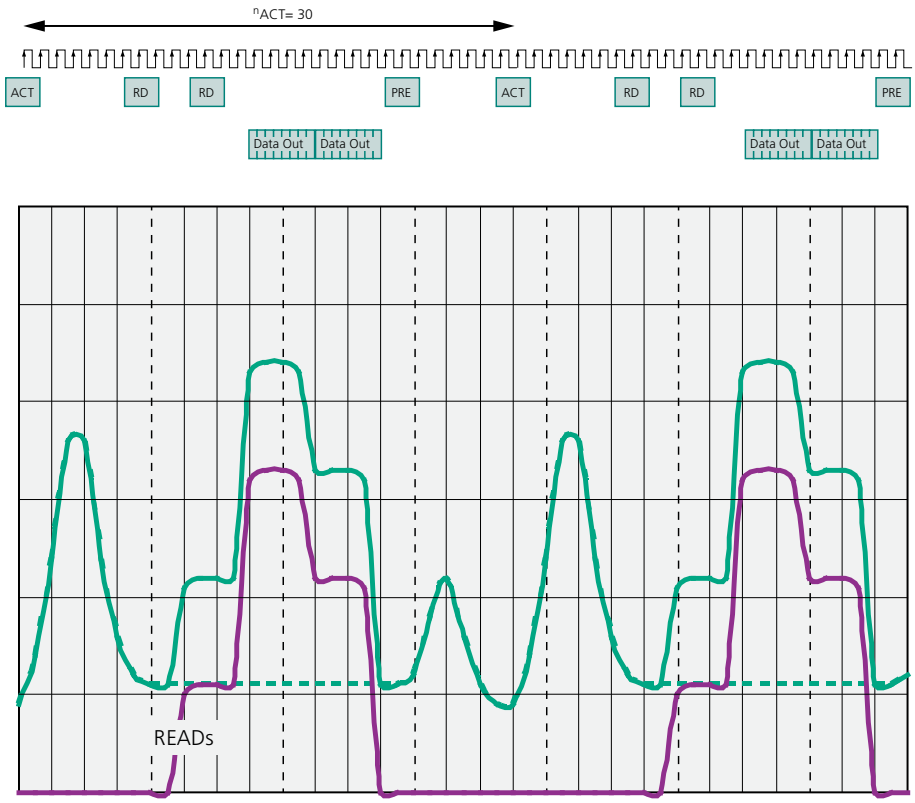
Table 19: Scaled Write Power – V_{PP} Supply

Formula	Equation
Pschp(WR) = Pdsp(WR) × WRsch% Pschp(WR) = 0mW × 22% **Pschp(WR) = 0mW**	15a

Read Power

The power required to read data is similar to that needed to write data, as shown in the following figure. A row is opened with an ACT command, and then a set of two BL = 8 READs is completed from columns in that row. After the READs are complete, the row is closed with a PRE command and the sequence is restarted.

Figure 8: Current Profile – READs



The read current profile looks very similar to the write current profile. The average current is calculated exactly the same as in the write case, except I_{DD4R} is substituted for I_{DD4W}.

Table 20: Base Read Power – V_{DD} Supply

Formula	Equation
Pds(RD) = (I_{DD4R} - I_{DD3N}) × V_{DD} Pds(RD) = (146mA - 46mA) × 1.26V **Pds(RD) = 126mW**	16

Table 21: Base Read Power – V_{PP} Supply

Formula	Equation
Pdsp(RD) = (I_{PP4R} - I_{PP3N}) × V_{PP} Pdsp(RD) = (3mA - 3mA) × 2.75V **Pdsp(RD) = 0mW**	16a

To scale the data sheet power to actual power based on command scheduling, it must be calculated as a ratio of the read bandwidth. This is denoted as RDsch%, which is the total number clock cycles containing read data (not READ commands) that are on the data bus versus the total number of clock cycles. The RDsch% calculation is shown in Equation 17.

Table 22: Scaling Read Power – V_{DD} and V_{PP} Supply

Formula	Equation
RDsch% = Num_of_read_cycle / *n*ACT RDsch% = 8 cycles / 32*n*CK **RDsch% = 25%**	17

After the ratio of READs is known, the power associated with the scheduled READs, Psch(RD), can be easily calculated from the data sheet read power in Equation 18.

Table 23: Scaled Read Power – V_{DD} Supply

Formula	Equation
Psch(RD) = Pds(RD) × RDsch% Psch(RD) = 126mW × 25% **Psch(RD) = 31.5mW**	18

Table 24: Scaled Read Power – V_{PP} Supply

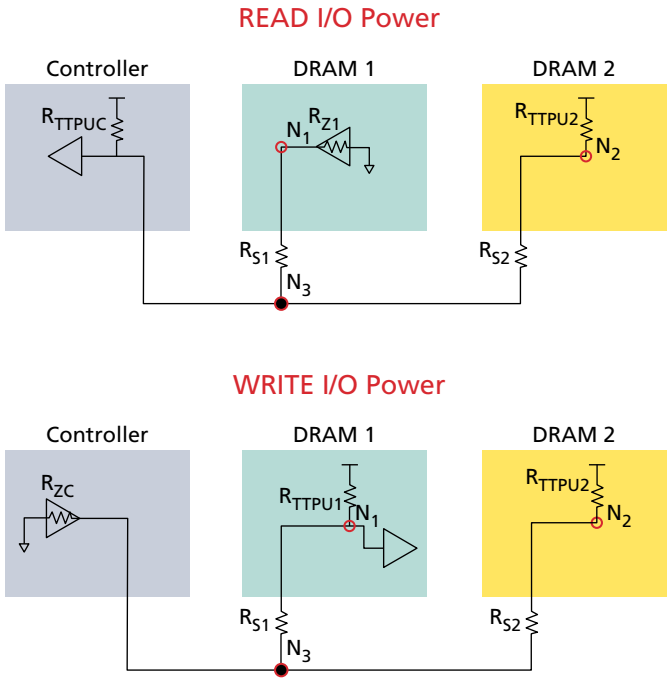
Formula	Equation
Pschp(RD) = Pdsp(RD) × RDsch% Pschp(RD) = 0mW × 25% **Pschp(RD) = 0mW**	18a

I/O Termination Power

Psch(RD) and Psch(WR) are only part of the total power for read and write sequences. Data sheet specifications do not include output driver power or ODT power. These powers are system-dependent and must be calculated for each system.

DDR4 systems can vary greatly depending on the application's density and form factor requirements. A typical small density system is shown in the following figure. The data bus connects the controller to two DDR4 SDRAM. Additionally, the controller and the DRAM utilize ODT for the data lines so no external passive components are required for this example system.

Figure 9: Typical System DQ Termination



The drivers in the system have an impedance of R_{ON}, which pulls the bus towards V_{DDQ} for a 1 or V_{SSQ} for a 0. The termination on the die is functionally a pull-up resistor.

A simple termination scheme for the example system is shown in the table below.

Table 25: Termination Configuration

	Controller		DRAM 1		DRAM 2	
	R_{ON}	R_{TT}	R_{ON}	R_{TT}	R_{ON}	R_{TT}
WRITEs to DRAM 1	34W	Off	Off	80W	Off	48W
READs from DRAM 1	Off	60W	34W	Off	Off	48W
WRITEs to DRAM 2	34W	Off	Off	48W	Off	80W
READs from DRAM 2	Off	60W	Off	48W	34W	Off

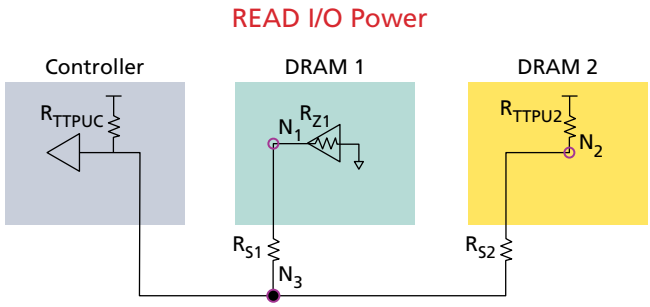
Two methods can be used to calculate the power consumed by the output driver and ODT. One is to simulate the system data bus using SPICE models of the components and then average the power consumed over a sufficiently long pattern of pseudo-random data. A simpler method, however, is to calculate the DC power of the output driver against the termination. This is usually not worst-case, but it provides a first-order approximation of the output power.

The I/O powers that must be calculated are:

- PdqRD: The output driver power when driving the bus
- PdqWR: The termination power when terminating a WRITE to the DRAM
- PdqRDoth: The termination power when terminating a READ from another DRAM
- PdqWRoth: The termination power when terminating write data to another DRAM

The nominal DRAM I/O termination DC power for the memory system can be calculated using Thevenin equivalent circuits (see the following two figures). The resultant I/O termination DC power values for the DRAM, per I/O pin, are listed in the following table. The controller and board series termination powers are not accounted for in the DRAM I/O termination power values even though they are shown for reference.

Figure 10: DRAM READ



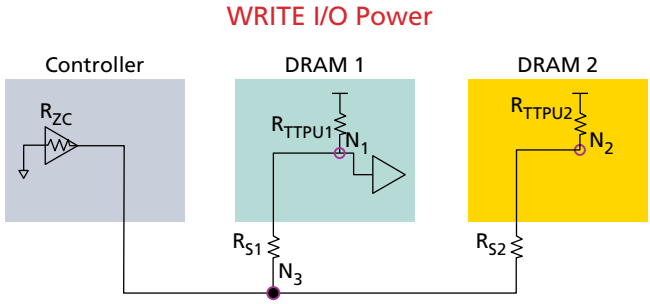
Enter values in dark blue boxes below — 0 = Disabled

RTTuC=	60	Rz1=	34	RTTu2=	48
		Rs1=	10	Rs2=	10

Calculated values in green boxes below

N3= (mV)	718	N1= (mV)	555	N2= (mV)	801
RTTuC= (mV)	3.9	Rz= (mV)	9.06	RTTd2= (mV)	3.31
		Rs1= (mV)	2.67	Rs2= (mV)	0.69
		pdqRD	11.73	pdqRDoth	4.00

Figure 11: DRAM WRITE



Enter values in dark blue boxes below — 0 = Disabled

RzC=	34	RTTu1=	80	RTTu2=	48
		Rs1=	10	Rs2=	10

Calculated values in green boxes below

N3= (mV)	589	N1= (mV)	657	N2= (mV)	694
RzC= (mV)	10.2	RTTPUd1= (mV)	3.69	RTTPUd2= (mV)	5.33
		Rs1= (mV)	0.46	Rs2= (mV)	1.11
		pdqWR	4.15	pdqWRoth	6.44

Table 26: Nominal I/O Termination Power Consumption

	DC Power	
	DRAM 1	DRAM 2
DRAM READ	pdqRD = 11.73mW / DQ	pdqRDoth = 4.0mW / DQ
DRAM WRITE	pdqWR = 4.15mW / DQ	pdqWRoth = 6.44mW / DQ

To calculate the power for output or termination on the DRAM, the power per DQ must be multiplied by the number of DQ and strobes on the device (num_DQR). For write termination, data masks must also be included in the sum of the total number of write signals that must be terminated (num_DQW). This will vary depending on data width of the DRAM. V_{PP} is not affected the I/O and termination power and does not require attention.

Equation 19 calculates the DRAM power for the following four I/O buffer operations:

- Pds(DQ): DRAM output driver power when driving the bus
- Pds(termW): DRAM termination power when terminating a WRITE to the DRAM
- Pds(termRoth): DRAM termination power when terminating a READ from another DRAM
- PPds(termWoth): DRAM termination power when terminating write data to another DRAM

Table 27: Termination Power – V_{DD} Supply

Formula	Equation
Pds(DQ) = Pdq(RD) × num_DQR Pds(termW) = Pdq(WR) × num_DQW Pds(termRoth) = Pdq(RDoth) × num_DQR Pds(termWoth) = Pdq(WRoth) × num_DQW	19

To illustrate how the power is calculated, an assumption using a x8 device is shown. For this example, num_DQR includes eight DQ and two DQS signals for a total of 10, whereas num_DQW totals 11 to account for the addition of the data mask. The DC power values from the Nominal I/O Termination Power Consumption table above are also used, and the results are presented in Equation 20.

Table 28: Termination Power – V_{DD} Supply

Formula	Equation
Pds(DQ) = 11.73mW × 10 = 117.3mW Pds(termW) = 4.15mW × 11 = 45.6mW Pds(termRoth) = 4.0mW × 10 = 40mW Pds(termWoth) = 6.44mW × 11 = 70.8mW	20

To complete the I/O and termination power calculation, the 100 percent usage data sheet specification must be derated based on the data bus utilization. The read and write utilization has already been provided as RDschd% and WRschd%. Two additional terms are required to cover the termination case for data to/from another DRAM. These are termRDsch% (terminating read data from another DRAM) and termWRsch% (terminating write data to another DRAM). The power based on command scheduling is then calculated as shown in the following table.

Table 29: Termination Power – V_{DD} Supply

Formula	Equation
Psch(DQ) = Pds(DQ) × RDsch% Psch(termW) = Pds(termW) × WRsch% Psch(termRoth) = Pds(termRoth) × termRDsch Psch(termWoth) = Pds(termWoth) × termWRsch	21

Sample calculations showing how to determine the output and termination percentages are provided in DDR4 Power Spreadsheet Usage Example.

Refresh Power

Refresh is the final power component that must be calculated for the device to retain data integrity. DDR4 memory cells store data information in small capacitors that lose their charge over time and must be recharged. The process of recharging these cells is called refresh.

The specification for refresh in the DDR4 data sheet is I_{DD5B}. I_{DD5B} assumes the DRAM is operating continuously at minimum REFRESH-to-REFRESH command spacing, ^{t}RFC (MIN). Some data sheets may use I_{DD5R} instead of I_{DD5B}, in which case I_{DD5R} can be

converted to I_{DD5B} by following Equation 100. If x4 data is available, calculate both x4 and x8 and use the larger of the two.

Table 30: Converting I_{DD5R} to I_{DD5B}

Formula	Equation
$I_{DD5B}(x4) = [(I_{DD5R} - I_{DD2N}) \times {}^{t}REFI / {}^{t}RFC] + I_{DD2N}$ $I_{DD5B}(x4) = [(56mA - 41mA) \times 7800ns / 350ns] + 41mA$ $I_{DD5B}(x4) = 375mA$	100
$I_{DD5B}(x8) = [(I_{DD5R} - I_{DD2N}) \times {}^{t}REFI / {}^{t}RFC] + I_{DD2N}$ $I_{DD5B}(x8) = [(56mA - 46mA) \times 7800ns / 350ns] + 46mA$ $I_{DD5B}(x8) = 269mA$	

Table 31: Converting I_{PP5R} to I_{PP5B}

Formula	Equation
$I_{PP5B}(x4) = [(I_{PP5R} - I_{PP2N}) \times {}^{t}REFI / {}^{t}RFC] + I_{PP2N}$ $I_{PP5B}(x4) = [(5mA - 3mA) \times 7800ns / 350ns] + 3mA$ $I_{PP5B}(x4) = 48mA$	100a
$I_{PP5B}(x8) = [(I_{PP5R} - I_{PP2N}) \times {}^{t}REFI / {}^{t}RFC] + I_{PP2N}$ $I_{PP5B}(x8) = [(5mA - 3mA) \times 7800ns / 350ns] + 3mA$ $I_{PP5B}(x8) = 48mA$	

During this operation, the DRAM is also consuming I_{DD3N} standby current. Thus, to calculate only the power due to refresh, I_{DD3N} must be subtracted, as shown in Equation 22.

Table 32: Refresh Power – V_{DD}

Formula	Equation
$Pds(REF) = (I_{DD5B} - I_{DD3N}) \times V_{DD}$ $Pds(REF) = (375mA - 46mA) \times 1.26V$ $Pds(REF) = 415mW$	22

Table 33: Refresh Power – V_{PP}

Formula	Equation
$Pdsp(REF) = (I_{PP5B} - I_{PP3N}) \times V_{PP}$ $Pdsp(REF) = (48mA - 3mA) \times 2.75V$ $Pdsp(REF) = 124mW$	22a

Table 34: Derating Refresh Power to Use Condition – V_{DD}

Formula	Equation
$Psch(REF) = Pds(REF) \times {}^{t}RFC (MIN) / {}^{t}REFI$ $Psch(REF) = 415mW \times 350ns / 7800ns$ $Psch(REF) = 18.6mW$	23

Table 35: Derating Refresh Power to Use Condition – V_{PP}

Formula	Equation
Pschp(REF) = Pds(REF) × ^{t}RFC (MIN) / ^{t}REFI Pschp(REF) = 124mW × 350ns / 7800ns Pschp(REF) = 5.5mW	23

Power Derating

Thus far, the power calculations have assumed a system operating at worst-case V_{DD}. They have also assumed the clock frequency in the system is the same as the frequency defined in the data sheet. The resulting power is denoted as Psch(XXX). Most systems, however, operate at different voltages or clock frequencies than the ones defined in the data sheet. Each of the power components must be derated to the actual system conditions, with the resulting power denoted as Psys(XXX).

The following section explains how to derate each of the power components to an actual system.

Voltage Supply Scaling

Most applications operate near the nominal V_{DD}, not at the absolute maximum V_{DD}. The only power parameters that do not scale with V_{DD} are the data I/O and termination power because the system V_{DD} is already assumed when the initial power is calculated.

On DRAM, power is typically related to the square of the voltage. This is because most of the power is dissipated by capacitance, with $P = CV^2f$ where C = internal capacitance, V = supply voltage and f = frequency of the clock or command (see Frequency Scaling). Thus, to scale power to a different supply voltage use Equations 24 and 24a.

Table 36: Scaling Voltage Supply – V_{DD}

Formula	Equation
Psys(XXX) = Psch(XXX) × (V_{DD} used / V_{DDmax} spec)^2	24

Table 37: Scaling Voltage Supply – V_{PP}

Formula	Equation
Psys(XXX) = Psch(XXX) × (V_{PP} used / V_{DDmax} spec)^2	24a

Frequency Scaling

Power components, such as Psch(PRE_PDN), Psch(ACT_PDN), Psch(ACT_STBY), Psch(PRE_STBY), Psch(WR), and Psch(RD), are dependent on the clock frequency at which a device operates and will scale with clock frequency. Psch(REF) does not scale with clock frequency, and Psch(ACT) is dependent on the interval between ACT commands, rather than clock frequency.

The power for components dependent on an operating frequency can be scaled for actual operating frequency using Equation 25.

Table 38: Scaling Clock Frequency

Formula	Equation
Psys(XXX) = Psch(XXX) × (freq_used / spec_freq)	25

The freq_used is the actual clock frequency at which a device operates in the system. The spec_freq is the clock frequency at which the device was tested during the IDD tests. This information is provided in the test condition notes in a data sheet. The test condition notes also describe tests at the minimum clock rate for a specific CAS latency, and that value is specified under the tCK parameter.

The combination of all V_{DD} and clock frequency scaling is presented in Equation 26.

Table 39: Clock Frequency and V_{DD} Supply Scaling

Formula	Equation
Psys(PRE_PDN) = Psch(PRE_PDN) × (freq_used / spec_freq) × (V_{DD} used / V_{DDmax} spec)^2 Psys(ACT_PDN) = Psch(ACT_PDN) × (freq_used / spec_freq) × (V_{DD} used / V_{DDmax} spec)^2 Psys(PRE_STBY) = Psch(PRE_STBY) × (freq_used / spec_freq) × (V_{DD} used / V_{DDmax} spec)^2 Psys(ACT_STBY) = Psch(ACT_STBY) × (freq_used / spec_freq) × (V_{DD} used / V_{DDmax} spec)^2 Psys(RD) = Psch(RD) × (freq_used / spec_freq) × (V_{DD} used / V_{DDmax} spec)^2 Psys(WR) = Psch(WR) × (freq_used / spec_freq) × (V_{DD} used / V_{DDmax} spec)^2 Psys(REF) = Psch(REF) × (V_{DD} used / V_{DDmax} spec)^2 Psys(ACT) = Psch(ACT) × (V_{DD} used / V_{DDmax} spec)^2	26

Table 40: Clock Frequency and V_{PP} Supply Scaling

Formula	Equation
Psysp(PRE_PDN) = Pschp(PRE_PDN) × (freq_used / spec_freq) × (V_{PP} used / V_{PPmax} spec)^2 Psysp(ACT_PDN) = Pschp(ACT_PDN) × (freq_used / spec_freq) × (V_{PP} used / V_{PPmax} spec)^2 Psysp(PRE_STBY) = Pschp(PRE_STBY) × (freq_used / spec_freq) × (V_{PP} used / V_{PPmax} spec)^2 Psysp(ACT_STBY) = Pschp(ACT_STBY) × (freq_used / spec_freq) × (V_{PP} used / V_{PPmax} spec)^2 Psysp(RD) = Pschp(RD) × (freq_used / spec_freq) × (V_{PP} used / V_{PPmax} spec)^2 Psysp(WR) = Pschp(WR) × (freq_used / spec_freq) × (V_{PP} used / V_{PPmax} spec)^2 Psysp(REF) = Pschp(REF) × (V_{PP} used / V_{PPmax} spec)^2 Psysp(ACT) = Pschp(ACT) × (V_{PP} used / V_{PPmax} spec)^2	26a

Calculating Total DRAM Power

The tools are now in place to calculate the system power for any usage condition. The last task is to put them together. The various system power subcomponents are summed together, as shown in Equation 27.

Table 41: Total DRAM Power – V_{DD}

Formula	Equation
Psys(TOT) = Psys(PRE_PDN) + Psys(PRE_STBY)+ Psys(ACT_PDN) + Psys(ACT_STBY) + Psys(WR)+ Psys(RD) + Psys(REF) + Psys(DQ)+ Psys(termW) + Psys(termRoth) + Psys(termWoth)	27

Table 42: Total DRAM Power – V_{PP}

Formula	Equation
Psysp(TOT) = Psysp(PRE_PDN) + Psysp(PRE_STBY)+ Psysp(ACT_PDN) + Psysp(ACT_STBY) + Psysp(WR) + Psysp(RD) + Psysp(REF) + Psysp(DQ)+ Psysp(termW) + Psysp(termRoth) + Psysp(termWoth)	27a

Having compensated for all primary variables that can affect device power, the total power dissipation of a DDR4 device operating under specific system usage conditions has now been calculated.

DDR4 Power Spreadsheet

Calculating all of these equations by hand can be tedious. For this reason, Micron has published an online worksheet to simplify the process. Micron's DDR4 SDRAM System-Power Calculator, as well as detailed instructions for its use, are available on Micron's web site at micron.com/systemcalc. An example of using the system-power calculator is provided in DDR4 Power Spreadsheet Usage Example.

To use the online spreadsheet, enter the device data sheet conditions on the "DDR4 Spec" tab. Starting values are provided, but it is important to verify all data sheet parameters prior to using the spreadsheet. Note that multiple speed bins and DRAM densities are included and that correct inputs are required for each column used.

After the data sheet values are entered, the actual DRAM configuration to be used for the power calculations is selected on the "DDR4 Config" tab, as shown in the following figure. The density, I/O configuration, speed grade, and if DBI is enabled or not are selected with pull-down menus. These inputs correctly configure the calculator for a specific DRAM based on the data input on the "DDR4 Spec" worksheet.

Figure 12: Spreadsheet – DRAM Configuration Tab

	DRAM Density	8Gb
MT/s	DRAM Width (Number of DQs per)	x8
2666	Speed Grade	-75E
	DBI Mode enabled	Off

After the DRAM configuration has been selected, the system operating conditions are input on the "System Config" tab, as shown in the following figure. The actual system operating V_{DD} and clock frequency are entered. Output power consumption and bus utilization are also entered, along with CKE conditions.

Figure 13: Spreadsheet – System Configuration Tab

	System VDD	1.2	V	
	System VPP	2.5	V	
	System CK frequency (data rate /2)	1333.3	MHz	DDR4-2666 Base
	Burst length	8		must be either BC 4 or BL8
PdqRD	DDR4 SDRAM output power per individual DQ on this DRAM during READs from this DRAM	11.73	mW	This value is the DRAM I/O power plus module series resistor power per DQ. The calculator to the right will estimate and populate the entries to the left
PdqWR	DDR4 SDRAM termination power per individual DQ during WRITEs to this DRAM	4.15	mW	
PdqRDoth	DDR4 SDRAM termination power per individual DQ during READs from other DRAM Rank*	4.00	mW	This value is the termination power plus module series resistor power per DQ. The calculator to the right will estimate and populate the entries to the left
PdqWRoth	DDR4 SDRAM termination power per individual DQ during WRITEs to other DRAM Rank*	6.44	mW	
BNK_PRE%	The percentage of time that all banks on the DRAM are in a precharged state	20.0%		
CKE_LO_PRE%	The percentage of the all bank precharge time for which CKE is held LOW	10%		
CKE_LO_ACT%	The percentage of the at least one bank active time for which CKE is held LOW	10%		
PH%	Page hit rate	50%		
RDsch%	The percentage of clock cycles which are outputting read data from the DRAM	25%		
WRsch%	The percentage of clock cycles which are inputting write data to the DRAM	15%		
termRDsch%	The percentage of clock cycles which are terminating read data to another DRAM Rank*	15%		
termWRsch%	The percentage of clock cycles which are terminating write data to another DRAM Rank*	25%		
	* must be 0% for a 1-rank system			
^{t}RRDsch*	The average time between ACT commands to this DRAM (includes ACT to same or different banks in the same DRAM device)	15	ns	

To assist calculating ^{t}RRDsch, one new parameter is added to this table that has not been previously discussed. This parameter is the PageHit% rate. The PageHit% is the percentage of READ and WRITE commands executed to an open row that has already been read from or written to divided by the total number of READ and WRITE commands. The PageHit% is application/system dependent. Desktop and notebook applications tend to have a high PageHit% while server and networking applications tend to have a very low PageHit%.

The PageHit% is used to calculated ^{t}RRDsch, as shown in Equation 28. Essentially the column-to-column time (CtC) is determined by: (^{t}CK × burstlength / 2) / (RD%+WR%). Then the ACT-to-ACT time, ^{t}RRDsch, is CtC / (100% - PH%).

Table 43: Page Hit Rate

Formula	Equation
^{t}RRDsch = [(^{t}CK × BL / 2) / (RDsch% + WRsch%)] / (1-page Hit%)	28

After all the inputs are entered, the actual DRAM device power derated to the system conditions can be found on the "Summary" tab. Note that the interim power calculations for data sheet power and scheduled power can also be found on the "Power Calcs" worksheet.

Data Sheet Specifications

Table 44: Data Sheet Assumptions for Micron's 8Gb DDR4-2666

Parameter/Condition		Symbol	-075E			Units
			x4	x8	x16	
Operating current: One bank active-precharge	V_{DD}	I_{DD0}	46	51	85	mA
	V_{PP}	I_{PP0}	3	3	4	mA
Precharge power-down current	V_{DD}	I_{DD2P}	25	25	25	mA
	V_{PP}	I_{PP2P}	3	3	3	mA
Precharge standby current	V_{DD}	I_{DD2N}	35	35	35	mA
	V_{PP}	I_{PP2N}	3	3	3	mA
Active power-down current	V_{DD}	I_{DD3P}	34	39	43	mA
	V_{PP}	I_{PP3P}	3	3	3	mA
Active standby current	V_{DD}	I_{DD3N}	41	46	50	mA
	V_{PP}	I_{PP3N}	3	3	3	mA
Operating burst read current	V_{DD}	I_{DD4R}	121	146	263	mA
	V_{PP}	I_{PP4R}	3	3	3	mA
Operating burst write current	V_{DD}	I_{DD4W}	112	132	244	mA
	V_{PP}	I_{PP4W}	3	3	3	mA
Burst refresh current, at ^{t}REFI	V_{DD}	I_{DD5R}	56	56	61	mA
	V_{PP}	I_{PP5R}	5	5	5	mA
Burst refresh current, at ^{t}RFC	V_{DD}	I_{DD5B}	375	375	375	mA
	V_{PP}	I_{PP5B}	48	48	48	mA

Notes:
1. I_{DD} is dependent on output loading, cycle rates, I_{OUT} = 0mA; ODT disabled.
2. Refer to the data sheet for the most current information and test conditions.

DDR4 Power Spreadsheet Usage Example

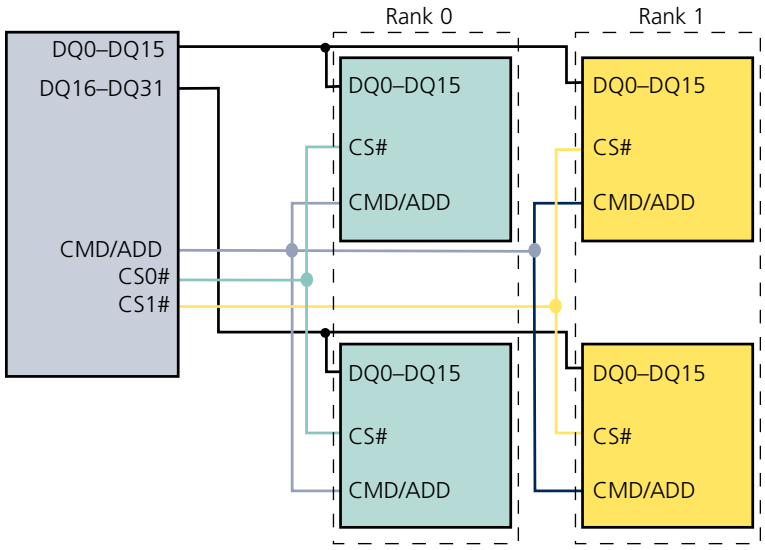
An example for calculating DDR4 power in a system environment is shown below. The system assumptions are for a two-rank system with a 32-bit data bus as shown in the following figure. This system is populated with 8Gb DDR4-2666 DRAM. The controller (shown in blue) drives a common command/address bus to all four DRAM. The DRAM are divided into two ranks with one rank shown in green and the second rank shown in

yellow. Each rank is driven by a unique chip select. DRAM are selected in a x16 I/O configuration to support the 32-bit controller data bus.

Total data bus for this example is 80% with read data utilizing 50% of the bandwidth and write data utilizing 30% of bandwidth. All data bus terminations follow the guidelines shown previously in the Termination Configuration table in the I/O Termination Power section. Because there are two ranks, it is assumed that each DRAM is accessed uniformly. However, the same power results can be obtained by applying one rank with all of the accesses and the second rank in standby in a dual-rank system.

To support this bandwidth, a burst length of eight is assumed with a page hit rate of 50%. Based on the high bus utilization, no CKE power management is assumed, and all banks precharged occurs only 20% of the time.

Figure 14: Mobile/Desktop System



Note: 1. Total data bus utilization = 80% (50% read data/30% write data).

To use the DDR4 Power Calculator spreadsheet, the I_{DD} data sheet values must be loaded into the "DDR4 Spec" tab. After these values are verified, the DRAM utilized in the system is selected using the pull-down menus on the "DRAM Config" tab as shown in the following figure.

Figure 15: DRAM Configuration

	DRAM Density	8Gb
MT/s	DRAM Width (Number of DQs per)	x16
2666	Speed Grade	-75E
	DBI Mode enabled	Off

After the DRAM is configured, the system implementation of the DRAM must be set using the "System Config" tab as shown in the following figure. The I/O and termination powers are system dependent. This example aligns to those calculated in the Nominal I/O Termination Power Consumption table in the I/O Termination Power section. Because this example system contains two ranks of memory, each DRAM rank is assumed

to consume half the total data bandwidth. Thus, each DRAM has a READ utilization of 25% and a WRITE utilization of 15%. The termination scheme also requires each DRAM to terminate the other DRAM's WRITE data bandwidth, which is also 15%.

With this information and the PageHit%, the spreadsheet calculates the average time between ACT commands of ^{t}RRDsch = 15ns.

Figure 16: System Configuration

	System VDD	1.2	V	
	System VPP	2.5	V	
	System CK frequency (data rate /2)	1333.3	MHz	DDR4-2666 Base
	Burst length	8		must be either BC 4 or BL8
PdqRD	DDR4 SDRAM output power per individual DQ on this DRAM during READs from this DRAM	11.73	mW	This value is the DRAM I/O power plus module series resistor power per DQ. The calculator to the right will estimate and populate the entries to the left
PdqWR	DDR4 SDRAM termination power per individual DQ during WRITEs to this DRAM	4.15	mW	
PdqRDoth	DDR4 SDRAM termination power per individual DQ during READs from other DRAM Rank*	4.00	mW	This value is the termination power plus module series resistor power per DQ. The calculator to the right will estimate and populate the entries to the left
PdqWRoth	DDR4 SDRAM termination power per individual DQ during WRITEs to other DRAM Rank*	6.44	mW	
BNK_PRE%	The percentage of time that all banks on the DRAM are in a precharged state	20.0%		
CKE_LO_PRE%	The percentage of the all bank precharge time for which CKE is held LOW	10%		
CKE_LO_ACT%	The percentage of the at least one bank active time for which CKE is held LOW	10%		
PH%	Page hit rate	50%		
RDsch%	The percentage of clock cycles which are outputting read data from the DRAM	25%		
WRsch%	The percentage of clock cycles which are inputting write data to the DRAM	15%		
termRDsch%	The percentage of clock cycles which are terminating read data to another DRAM Rank*	15%		
termWRsch%	The percentage of clock cycles which are terminating write data to another DRAM Rank*	25%		
	* must be 0% for a 1-rank system			
^{t}RRDsch*	The average time between ACT commands to this DRAM (includes ACT to same or different banks in the same DRAM device)	15	ns	

After all the assumptions are entered into the spreadsheet, it calculates each subcomponent of power and derates it to the system use condition. The results are shown on the "Summary" tab as shown in the Power Consumption Summary by Device figure that follows. During the system conditions, each DDR4 DRAM utilizes 85.5mW of power for background operations, 153.9mW of power for activating rows and 168.8mW of power for reading and writing data.

Therefore, each DRAM will consume approximately 408.3mW of total power. Because the calculations are completed on a per-DRAM basis, and the data was assumed to be uniformly distributed amongst all of the DRAM in the system, the total memory subsystem power can be approximated as four times 408.3mW, or 1.63W.

Figure 17: Power Consumption Summary by Device

	Total	VDD	VPP	
ACT	153.9	146.2	7.7	mW
Activate Power	153.9	146.2	7.7	mW
RD	64.6	63.96	0.7	mW
WR	35.3	34.9	0.4	mW
READ I/O	55.9	55.9	0.0	mW
Write ODT	13.0	13.0	0.0	mW
RD/WR/Term Power	168.8	167.8	0.0	mW
ACT_STBY	48.6	43.2	5.4	mW
PRE_STBY	8.9	7.6	1.4	mW
ACT_PDN	4.7	4.1	0.6	mW
PRE_PDN	0.8	0.6	0.2	mW
REF	22.5	17.5	5.0	mW
Background Power	85.5	73.0	12.5	mW
Total DDR4 SDRAM Power	408.3	387.0	21.2	mW
TERM 2nd rank	45.2	45.2	0.0	mW

Figure 18: Power Consumption per Device

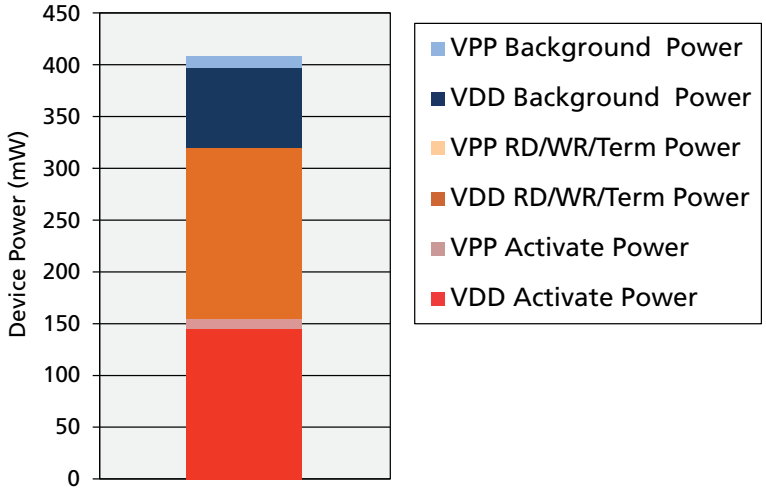
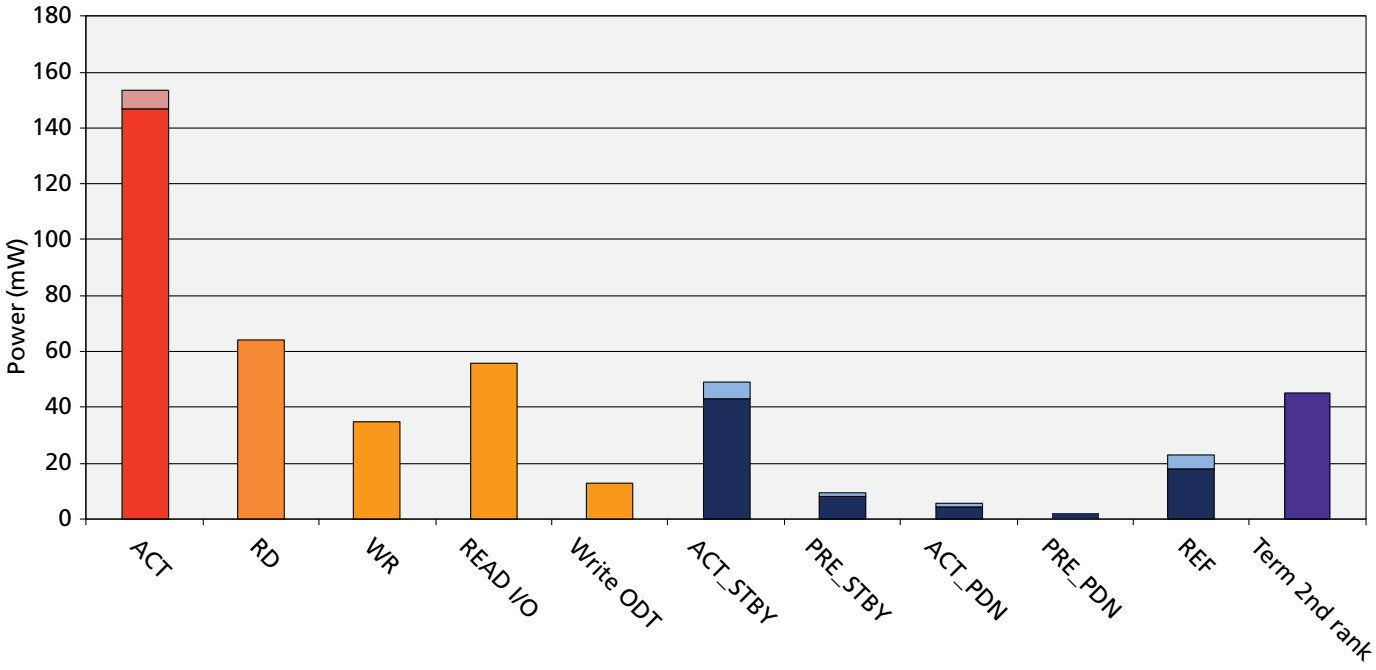


Figure 19: Power Consumption Breakout



Conclusion

When relying on a data sheet alone, it can be difficult to determine how much power a DDR4 device will consume in a system environment. However, by understanding the data sheet and how a DDR4 device consumes power, it is possible to create a power model based on system usage conditions. Such a model can enable system designers to experiment with various memory access schemes to determine the impact on power consumption — that is, more aggressive use of power-down (CKE = LOW) or changes to data access patterns (page hit percentages). In short, system designers can use this tool to estimate realistic power requirements for DDR4 devices and adjust a system's power delivery and thermal budget accordingly, optimizing system performance.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.