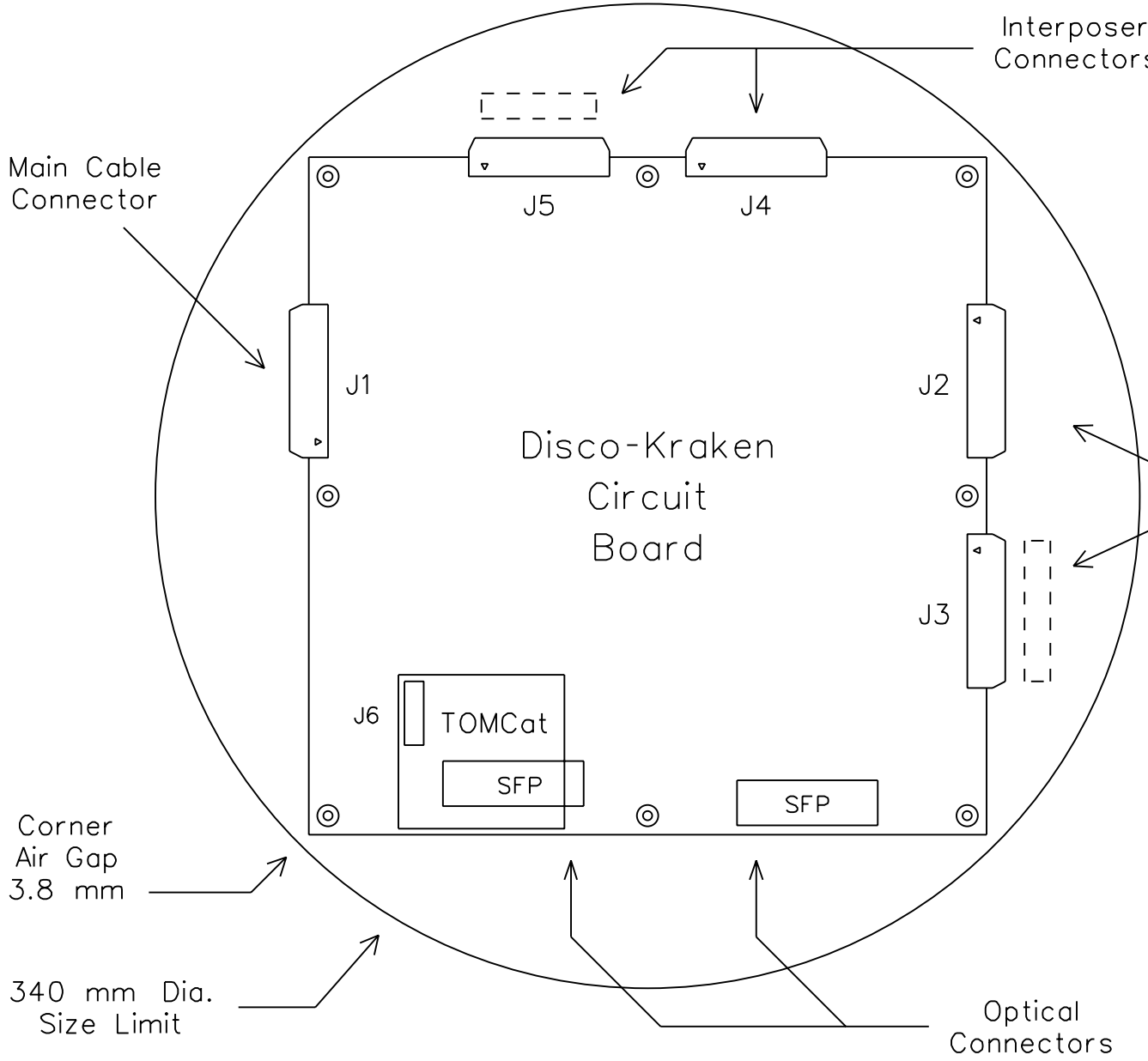
Disco-Kraken PCB Drawings Index - EPON Based

Rev. 5-Oct-2023

All DK board design files are available on the web:

https://web.pa.msu.edu/people/edmunds/Disco_Kraken/

Disco-Kraken - Board Size and Layout



DK Board Size:
235 mm Square

Vertical Space Available: 30 mm
4.0 mm Under PCB
2.5 mm PCB Thickness
22.5 mm Max Comp Height
1 mm Air Gap Above Max Comp

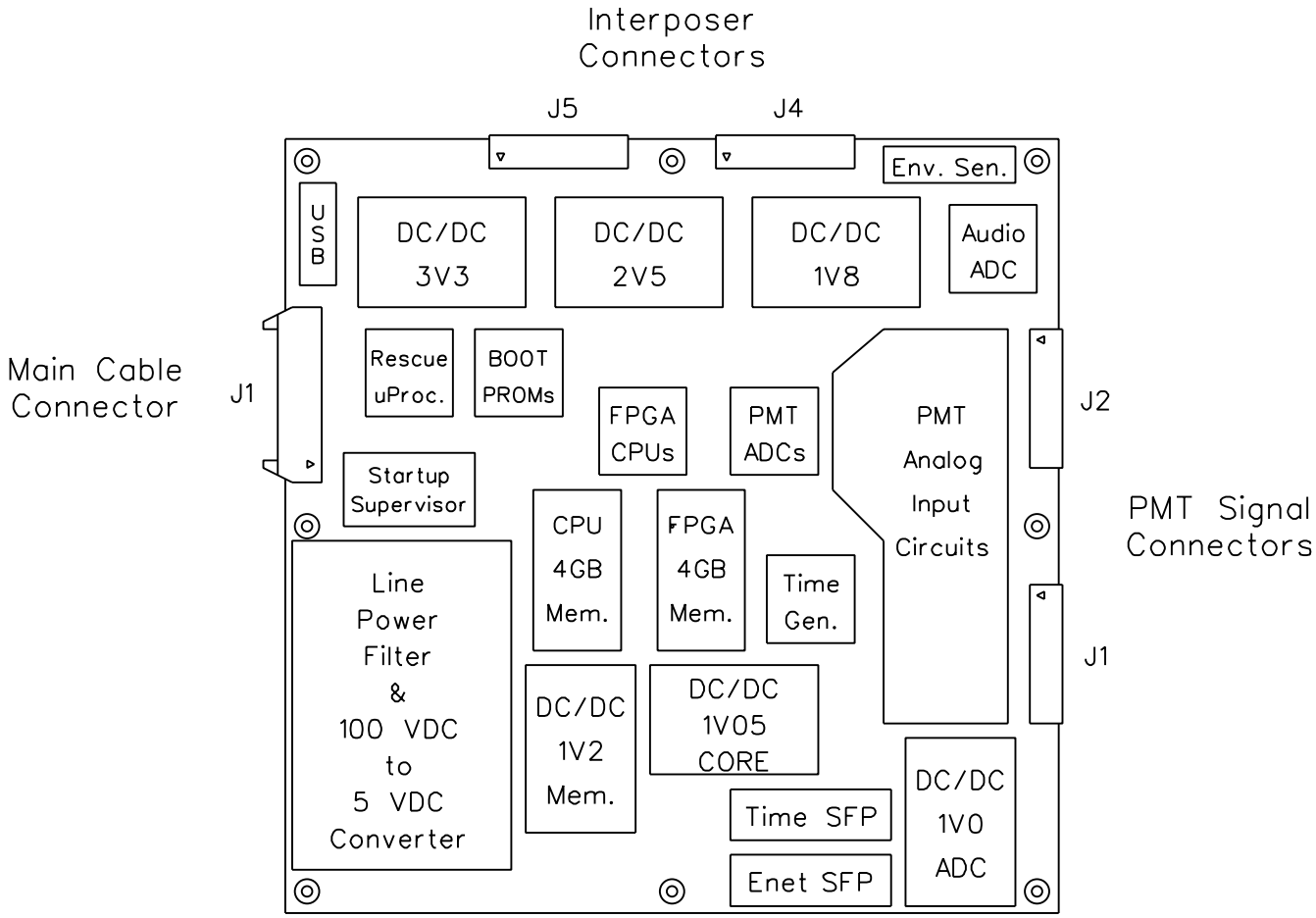
Slots in the Mounting Plate for the Cable Pass Throughs

Mounting Screws Set Back 6.0 mm from the Edge

100 mm

DK Drw. 26 Rev. 27-June-2023

Disco-Kraken - PCB Floor Plan



DK Board Size:
235 mm Square

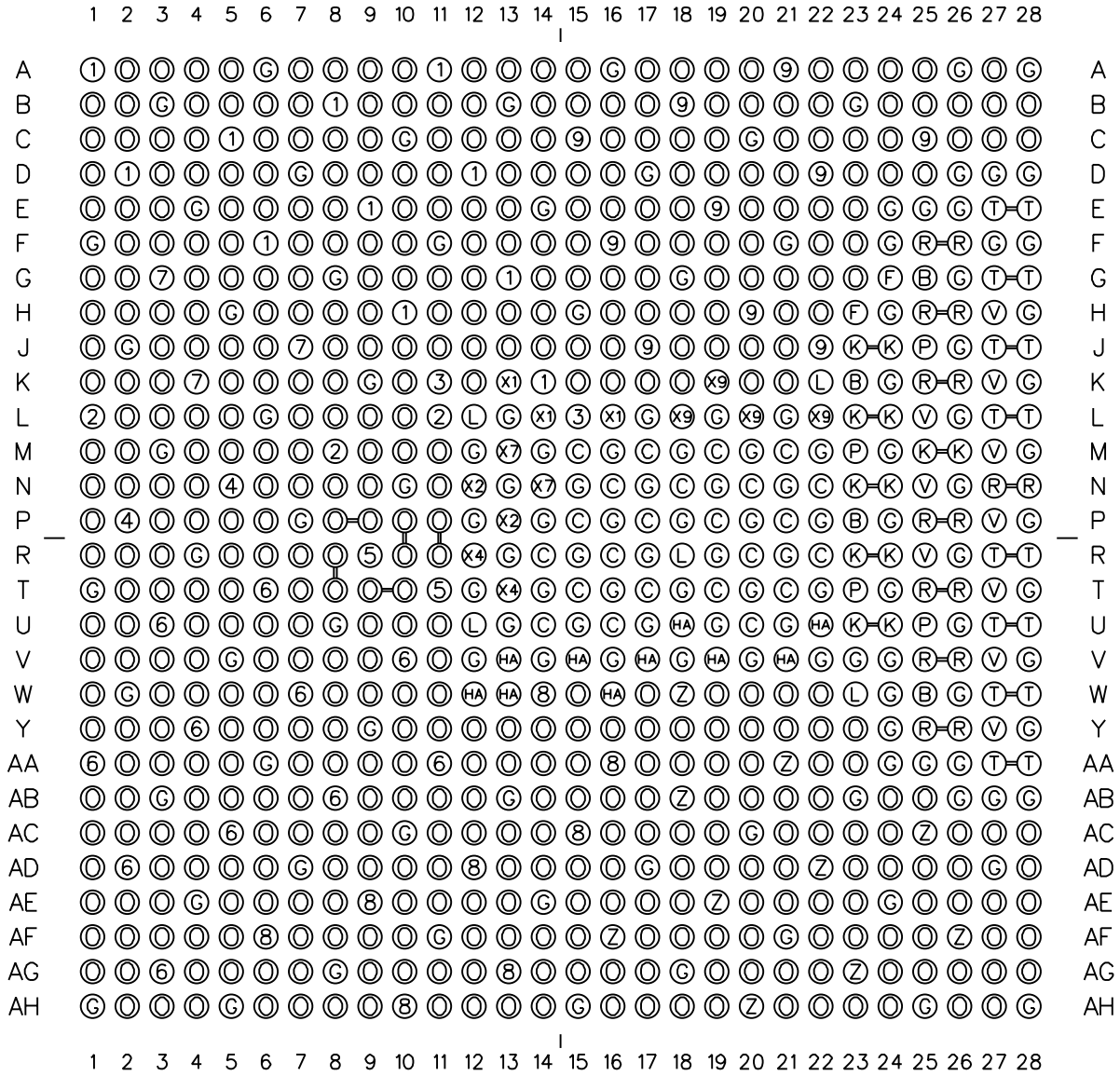
Vertical Space Available: 30 mm
4.0 mm Under PCB
2.5 mm PCB Thickness max
22.5 mm Max Comp Height
1 mm Air Gap Above Max Comp

The shown locations and areas are only the current estimates.

Many functions and connectors are not shown: 125 MHz crystal Oscillator, Barnacle Connector

◎ Mounting Screws

MPFS250T-1FCVG784I



C --> CORE 1V05

L --> PLL & PNVM 2V5

HA --> PROG & HSIO Aux 1V8

F --> XCVR Clk Ref 10k

B --> XCVR Clk Buf 2V5

P --> XCVR PLL 2V5

V --> XCVR Tx&Rx 1V05

T --> XCVR Tx Output

R --> XCVR Rx Input

K --> XCVR Clk Input

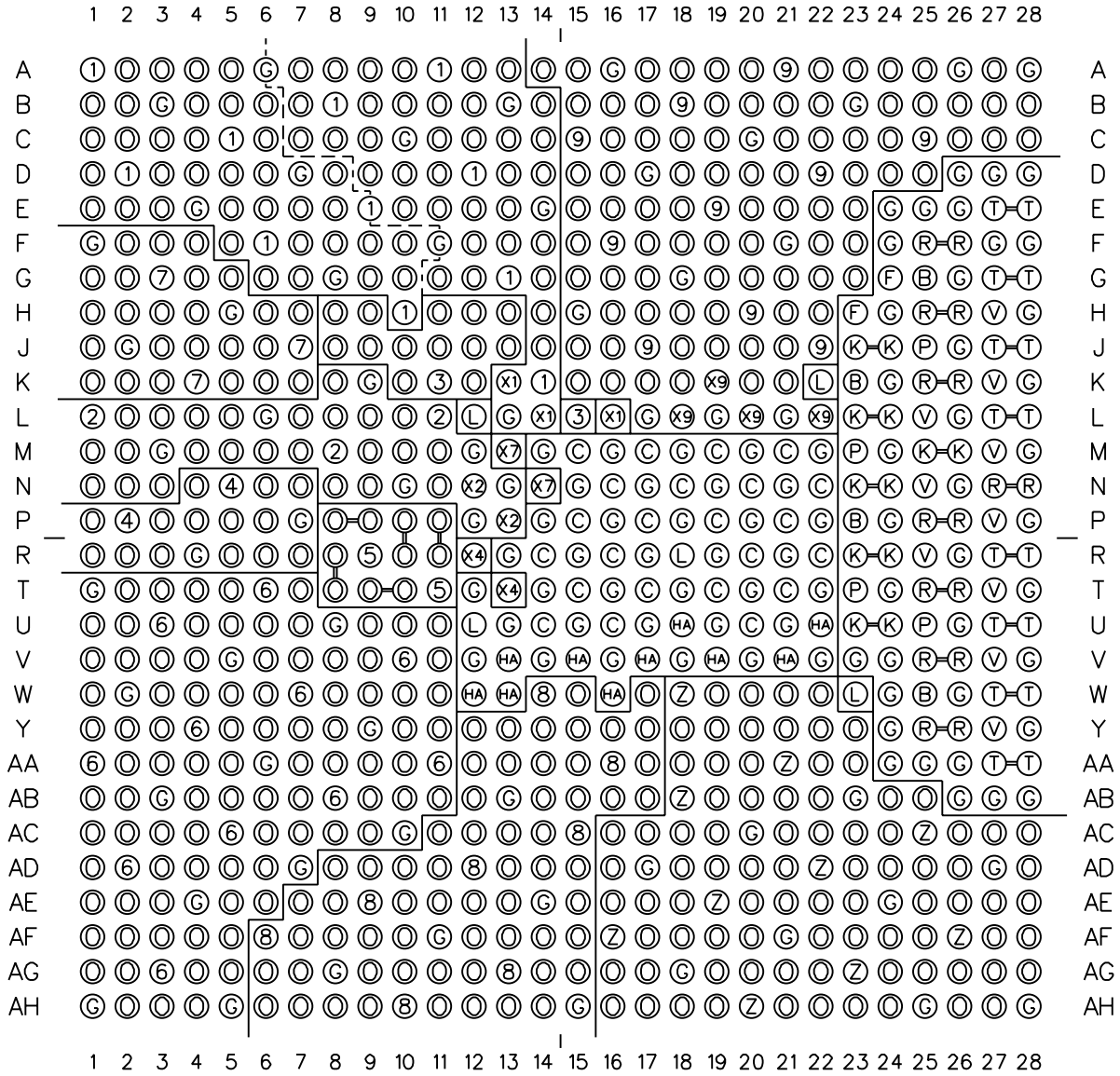
Z --> Bank 0 VDD

1:9 --> Banks 1:9 VDD

1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD

DK Drw. 25 Rev. 30-Aug-2023

MPFS250T-1FCVG784I I/O Banks



TOP VIEW

C --> CORE 1V05

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DK Drw. 61 Rev. 8-Sept-2023

FPGA/CPU - Power Bus Connections

DK SUPPLY	Microchip NAME	FUNCTION
CORE_1V05	VDD	Core Supply
DIGITAL_1V8	VDD18	Prgm & HSIO Aux
FPGA_PLL_2V5	VDD25	PLLs and PNVM
XCVR_1V05	VDDA	XCVR Power
XCVR_PLL_2V5	VDDA25	XCVR PLLs
XCVR_CLK_2V5	XCVR_CLK	XCVR Clk Buffers
10k Ohm to Gnd	XCVR_REF	XCVR Clk Ref.

DK SUPPLY		Microchip NAME	FUNCTION
BULK_1V2		VDDI0	I/O Bank 0 FPGA HSIO FPGA DDR4 Memory
BULK_3V3 BULK_3V3	*	VDDI1 VDDAUX1	I/O Bank 1 FPGA GPIO DK's 3V3 I/O
BULK_3V3 BULK_3V3	*	VDDI2 VDDAUX2	I/O Bank 2 CPU I/O USB UPLI & QSPI
BULK_3V3		VDDI3	I/O Bank 3 Controller JTAG & Controller SPI
10k Ohm Gnd 10k Ohm Gnd	*	VDDI4 VDDAUX4	I/O Bank 4 CPU I/O Not Used No Power
BULK_3V3		VDDI5	I/O Bank 5 CPU SGMII Used only for CPU Clk
BULK_1V2		VDDI6	I/O Bank 6 CPU DDR CPU DDR4 Memory
BULK_3V3 BULK_3V3	*	VDDI7 VDDAUX7	I/O Bank 7 FPGA GPIO If Used It's 3V3
10k Ohm Gnd		VDDI8	I/O Bank 8 FPGA HSIO Not Used No Power
DIGITAL_1V8 DIGITAL_2V5	*	VDDI9 VDDAUX9	I/O Bank 9 FPGA GPIO DK's 1V8 I/O

* When an FPGA GPIO Bank or a CPU IO Bank operates from 2V5 or 3V3 power then that Bank's Auxiliary supply must come from the same 2V5 or 3V3 bus.

* When an FPGA GPIO Bank or a CPU IO Bank operates from 1V8 or lower voltage power then that Bank's Auxiliary supply must come from the 2V5 bus.

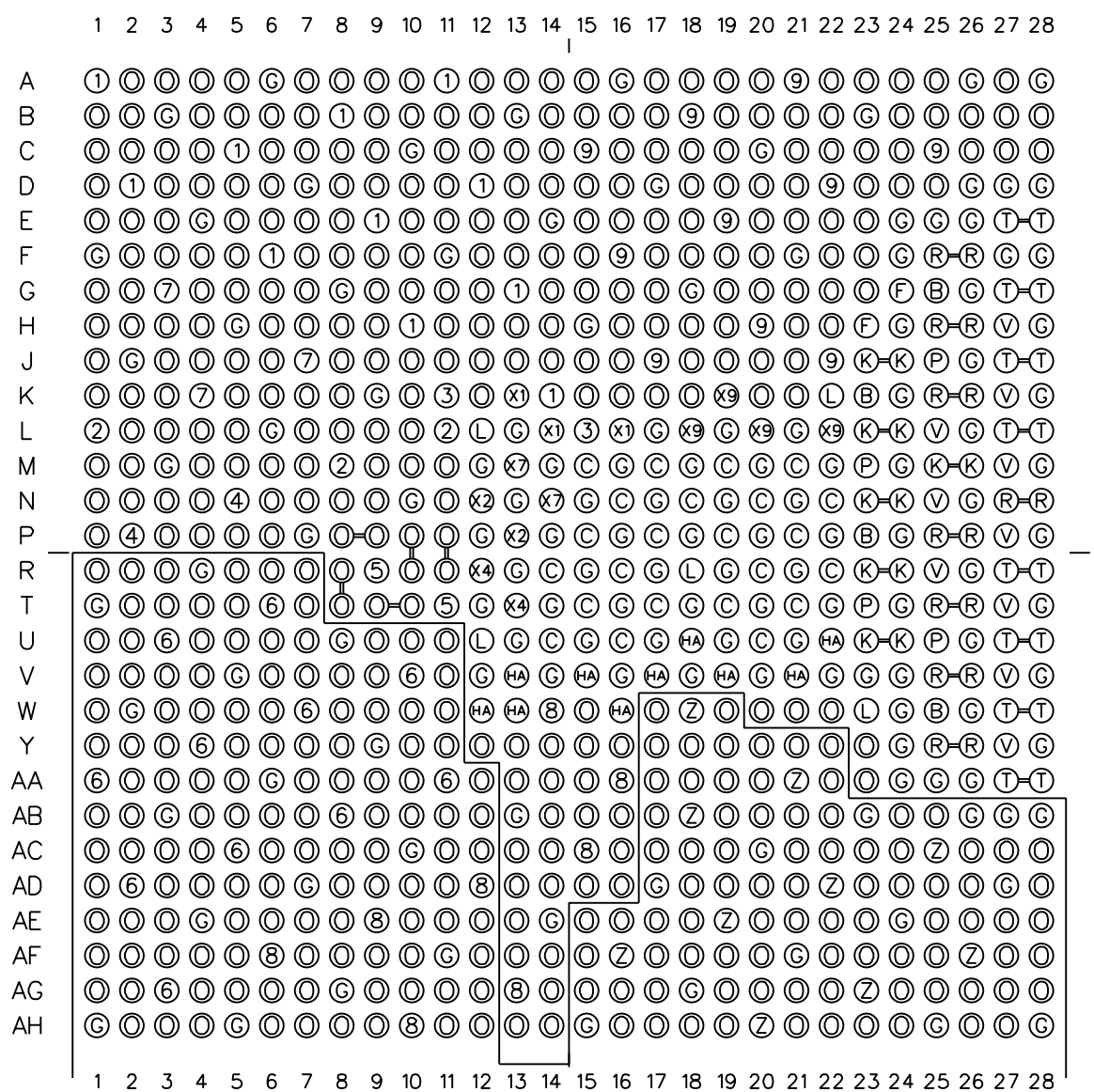
DK Drw. 45

Do not confuse VDD18 and VDDI8.

Rev. 1-Sept-2023

DK Board - FPGA/CPU - Minimum BULK_1V2 Plane

BULK_1V2 Connects to: I/O Banks 0 & 6 and DDR4 Memories



TOP VIEW

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R --> XCVR Rx Input

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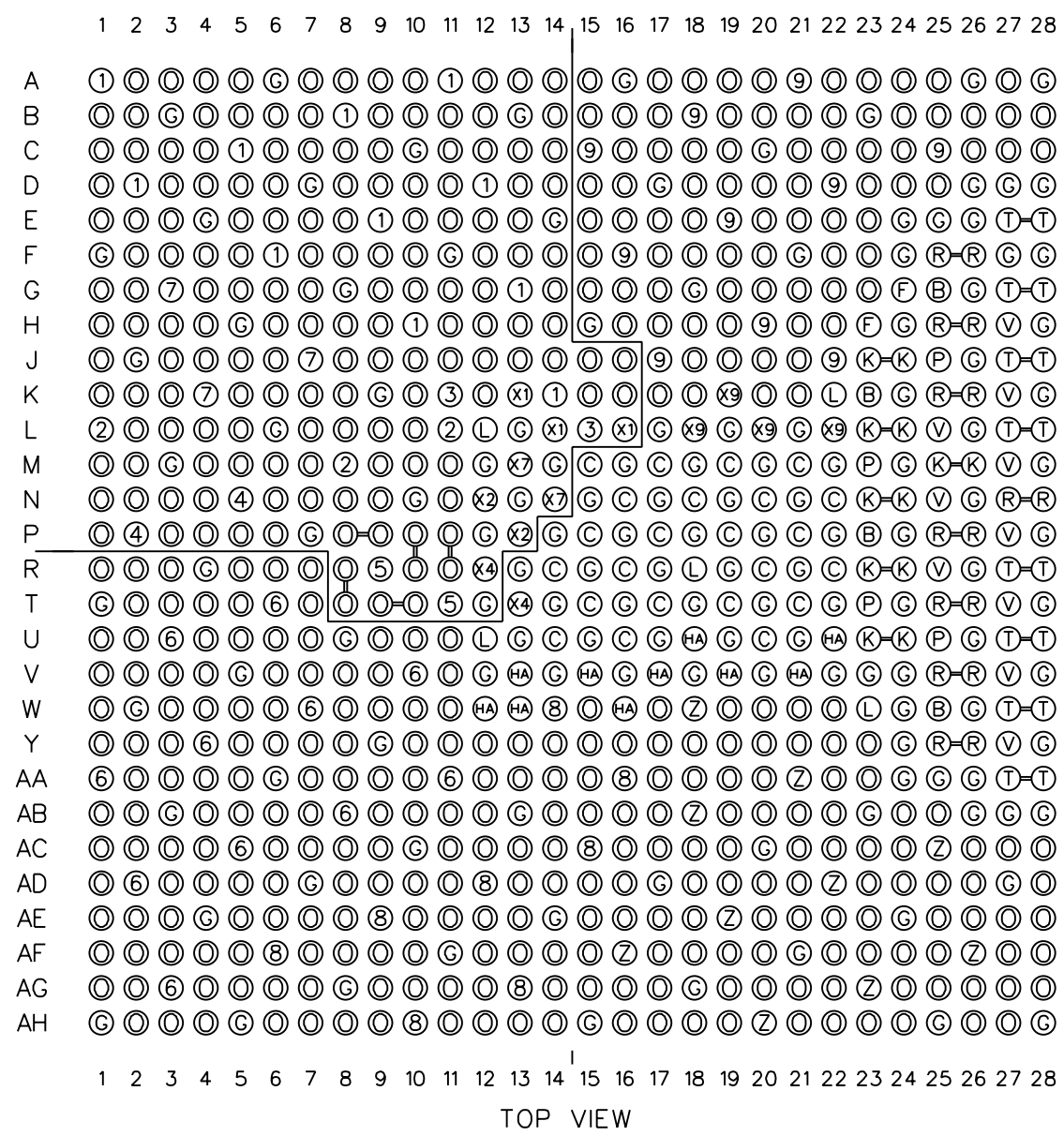
Z --> Bank 0 VDD

1:9 --> Banks 1:9 VDD

1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD

DK Board - FPGA/CPU - Minimum BULK_3V3 Plane

BULK_3V3 Connects to I/O Banks: 1, 1x, 2, 2x, 3, 5, 7, 7x



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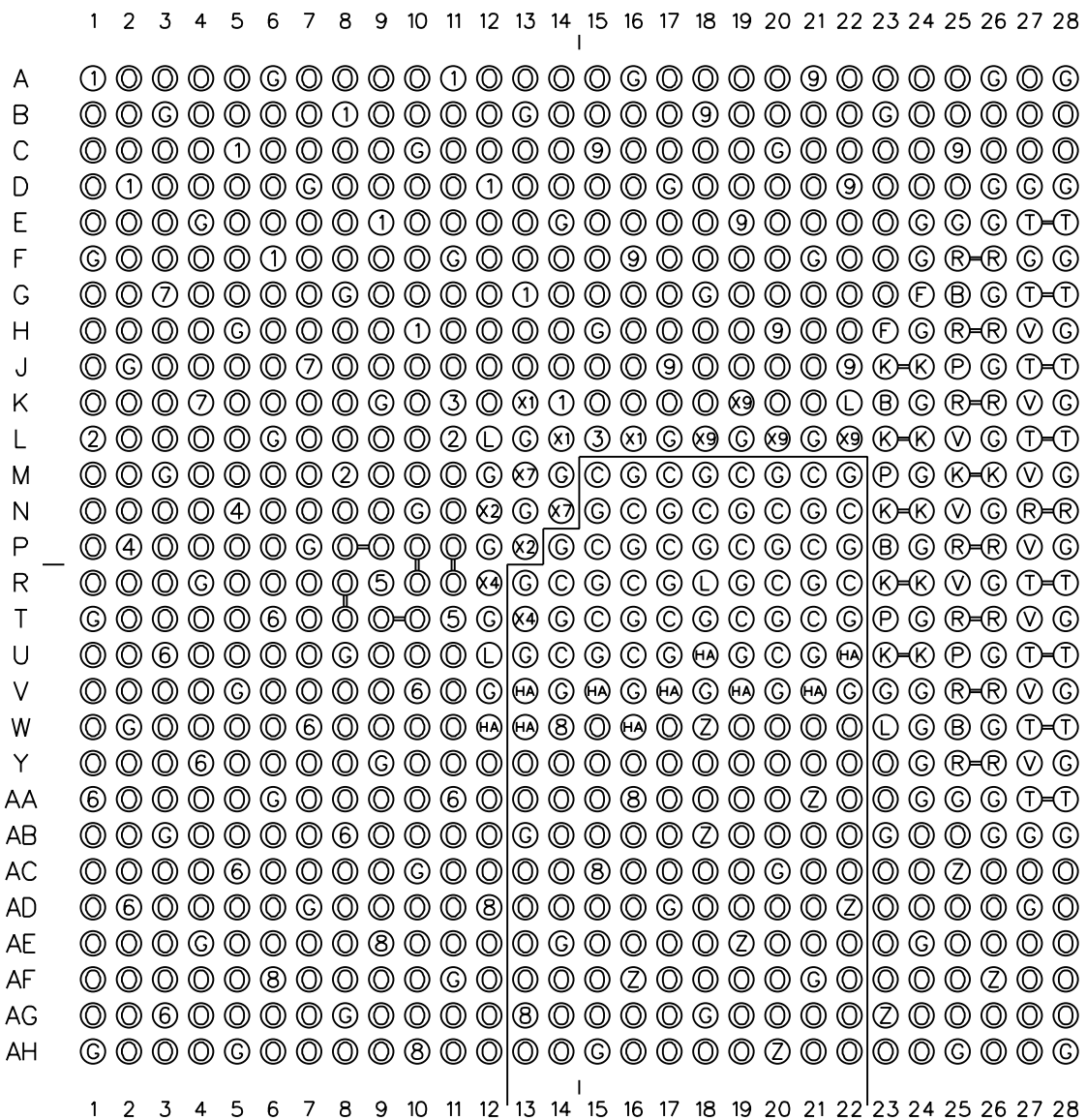
DK Board - FPGA/CPU - Minimum CORE_1V05 Plane

CORE_1V05 Connects to FPGA/CPU: CORE



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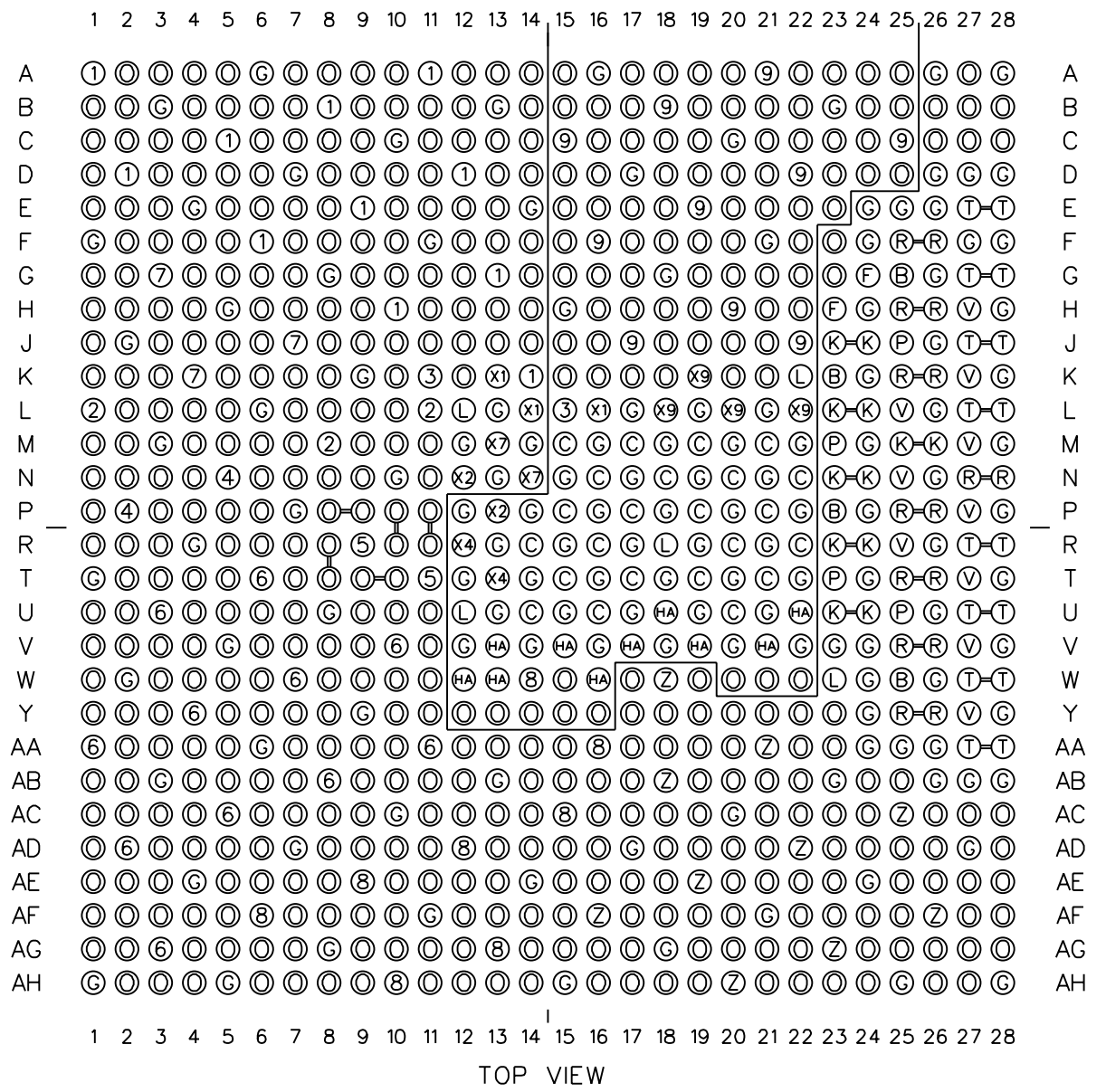
DK Board - FPGA/CPU - Minimum DIGITAL_1V8 Plane

DIGITAL_1V8 Connects to: VDD18 and I/O Bank_9



C --> CORE 1V05

L --> PLL & PNVM 2V5

HA --> PROG & HSIO Aux 1V8

F --> XCVR Clk Ref 10k

B --> XCVR Clk Buf 2V5

P --> XCVR PLL 2V5

V --> XCVR Tx&Rx 1V05

T --> XCVR Tx Output

R --> XCVR Rx Input

K --> XCVR Clk Input

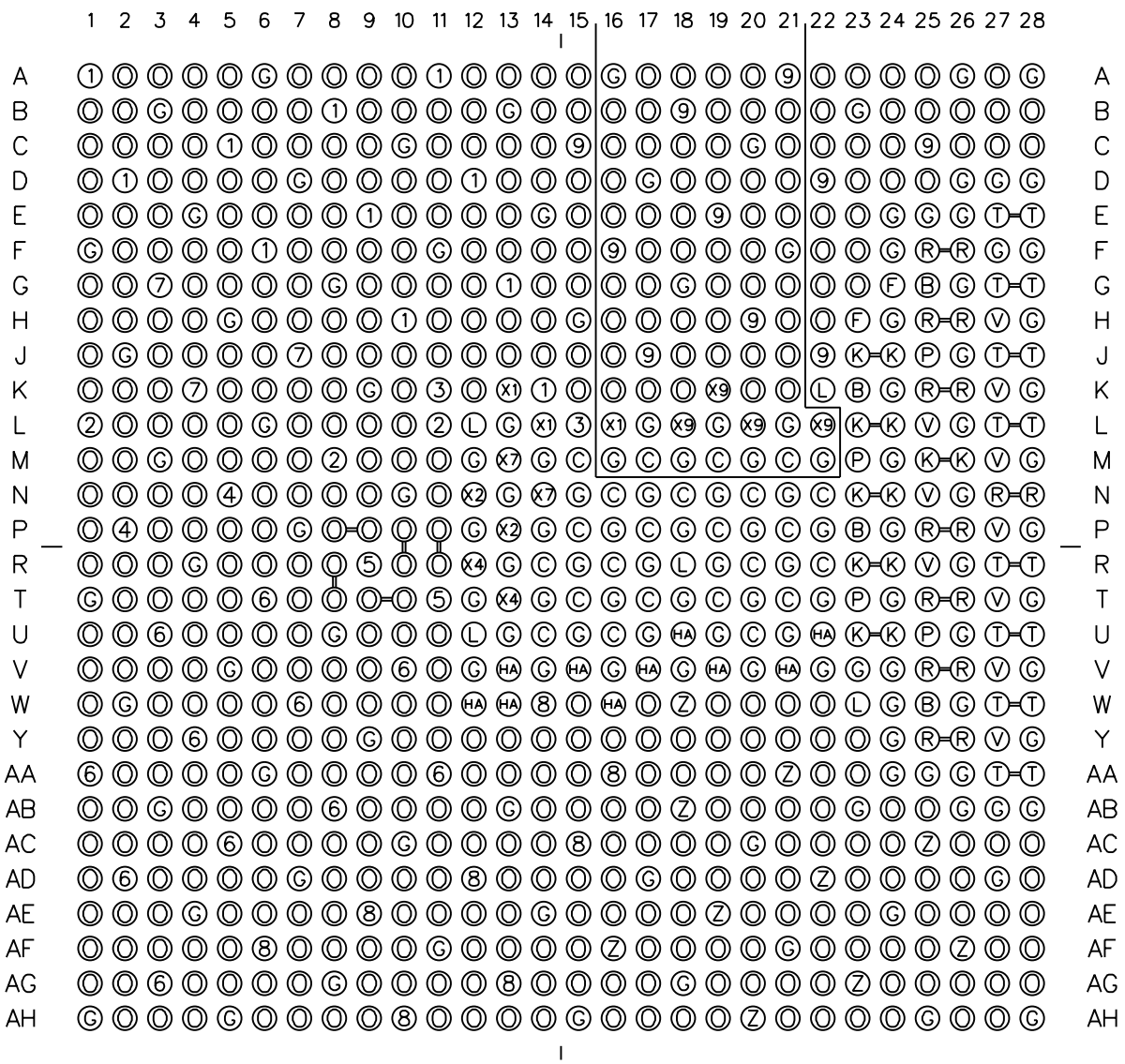
Z --> Bank 0 VDD

1:9 --> Banks 1:9 VDD

1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD

DK Board - FPGA/CPU - Minimum DIGITAL_2V5 Plane

DIGITAL_2V5 Connects to: VDDAUX for I/O BANK 9



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L --> PLL & PNVM 2V5

HA --> PROG & HSIO Aux 1V8

F --> XCVR Clk Ref 10k

B --> XCVR Clk Buf 2V5

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T --> XCVR Tx Output

R --> XCVR Rx Input

K --> XCVR Clk Input

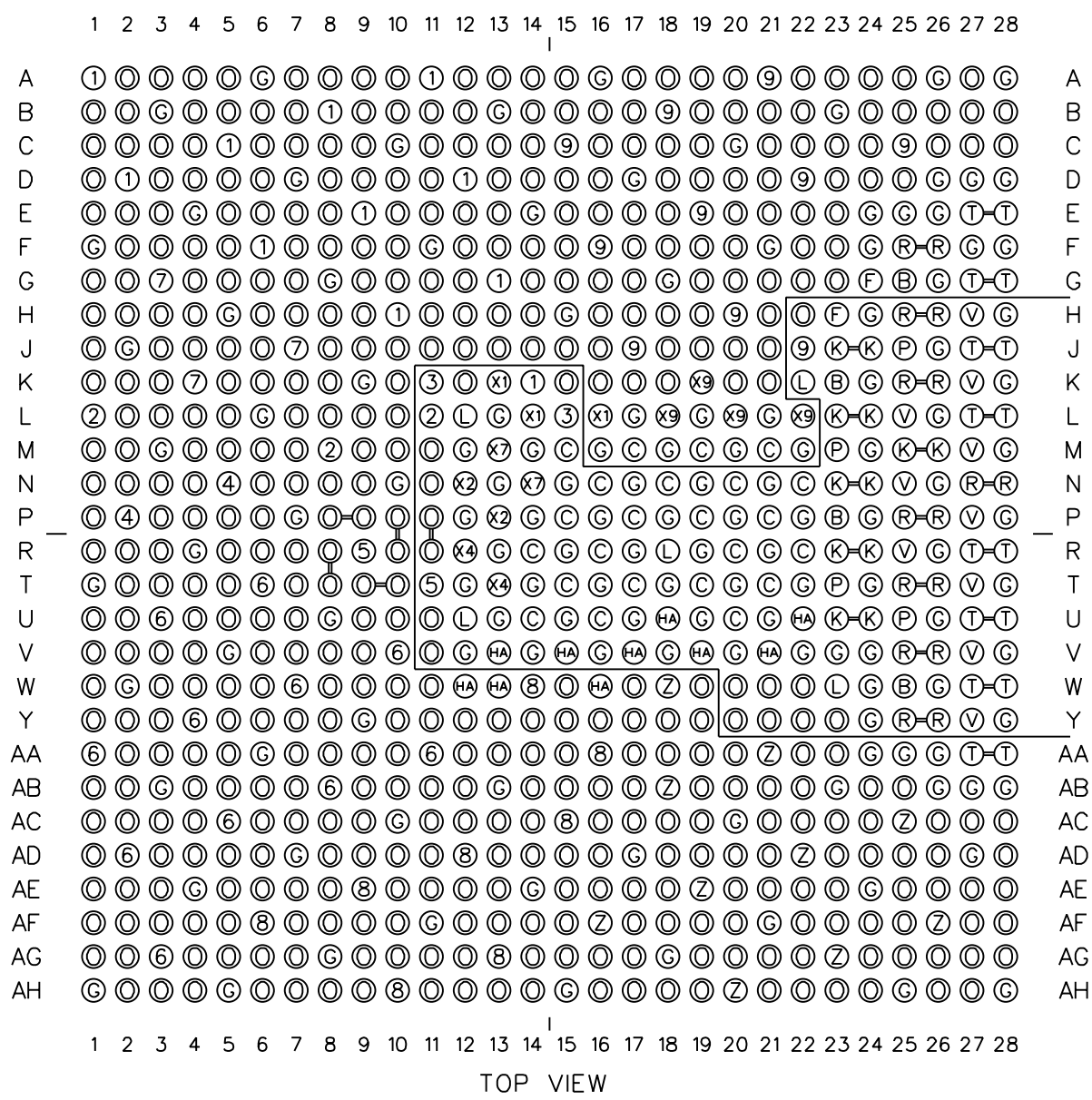
Z --> Bank 0 VDD

1:9 --> Banks 1:9 VDD

1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD

DK Board - FPGA/CPU - Minimum FPGA_PLL_2V5 Plane

FPGA_PLL_2V5 Connects to FPGA/CPU: VDD25



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HA --> PROG & HSIO Aux 1V8

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B --> XCVR Clk Buf 2V5

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T --> XCVR Tx Output

R --> XCVR Rx Input

K --> XCVR Clk Input

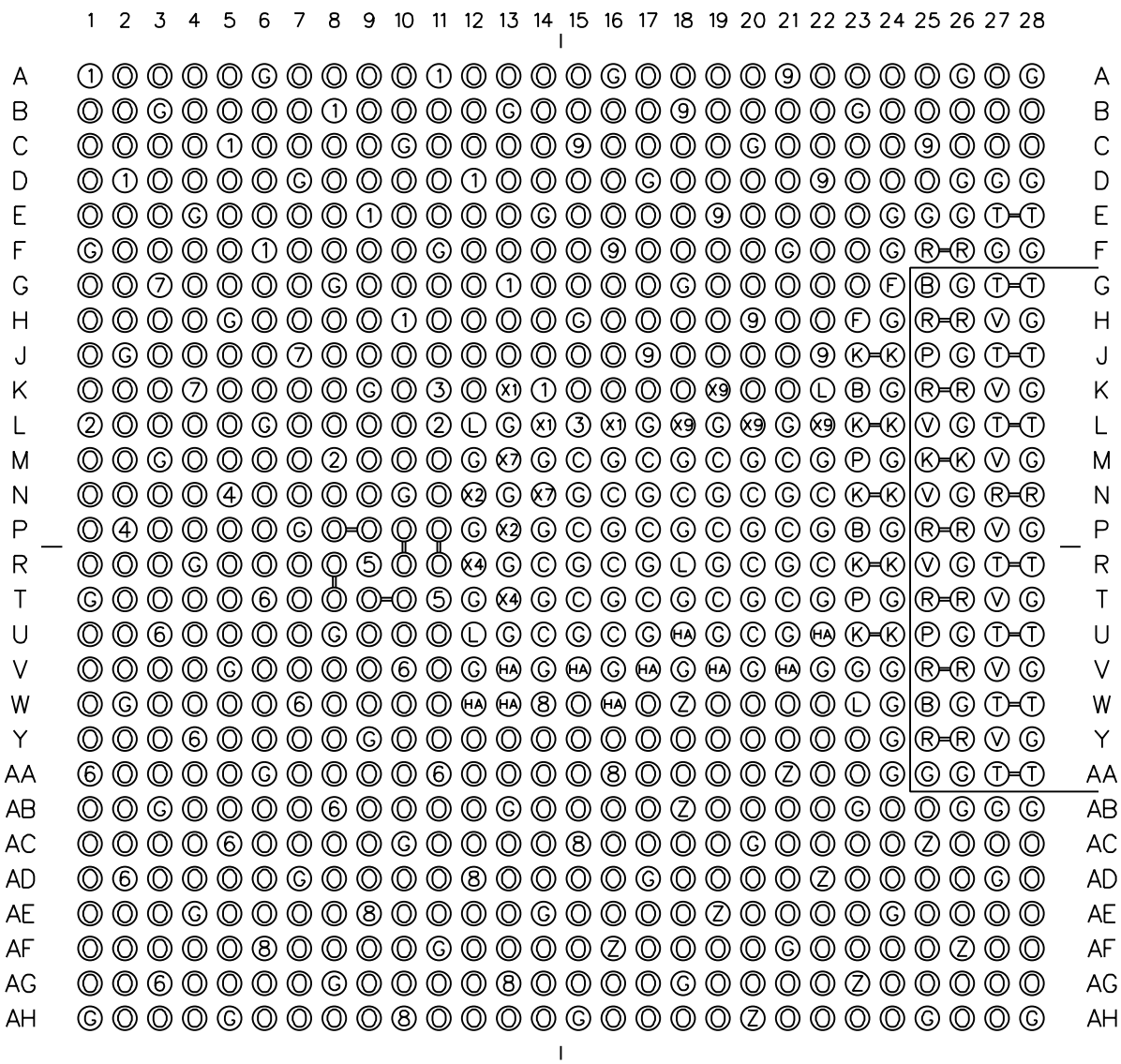
Z --> Bank 0 VDD

1:9 --> Banks 1:9 VDD

1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD

DK Board - FPGA/CPU - Minimum XCVR_1V05 Plane

XCVR_1V05 Connects to FPGA/CPU: VDDA



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HA --> PROG & HSIO Aux 1V8

F --> XCVR Clk Ref 10k

B --> XCVR Clk Buf 2V5

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T --> XCVR Tx Output

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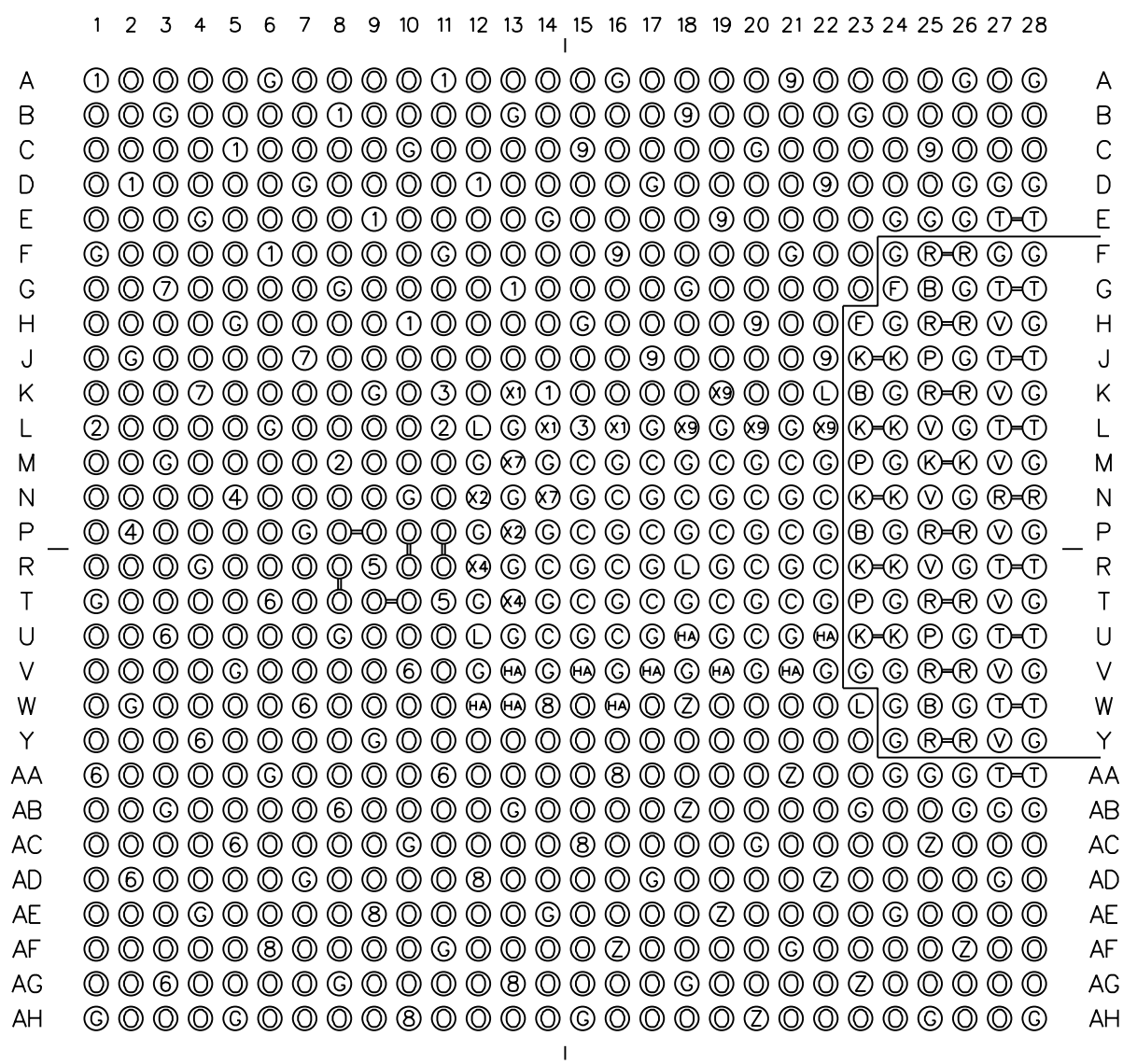
Z --> Bank 0 VDD

1:9 --> Banks 1:9 VDD

1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD

DK Board - FPGA/CPU - Minimum XCVR_CLK_2V5 Plane

XCVR_CLK_2V5 Connects to FPGA/CPU: XCVR_CLK



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T --> XCVR Tx Output

R --> XCVR Rx Input

K --> XCVR Clk Input

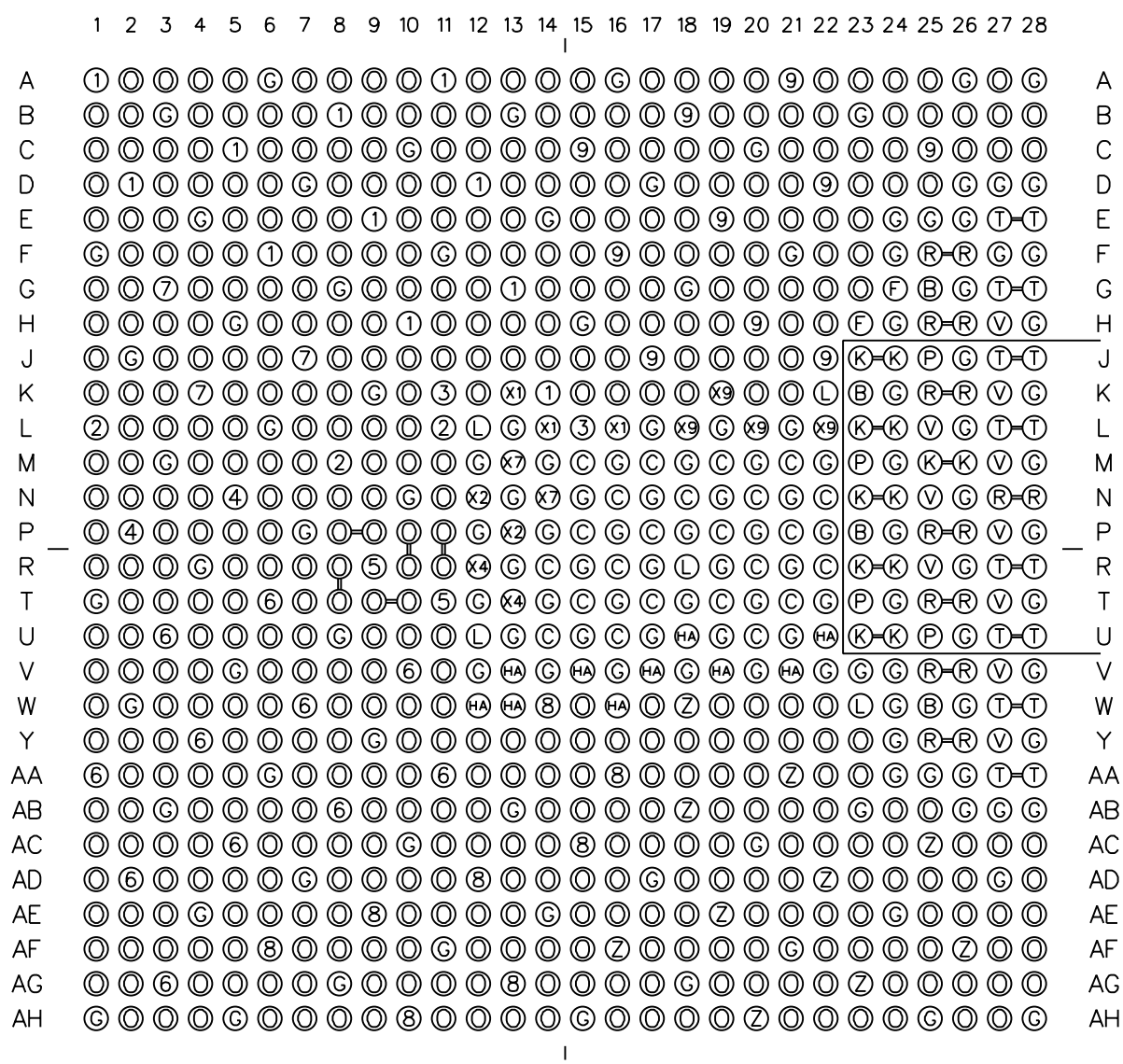
Z --> Bank 0 VDD

1:9 --> Banks 1:9 VDD

1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD

DK Board - FPGA/CPU - Minimum XCVR_PLL_2V5 Plane

XCVR_PLL_2V5 Connects to FPGA/CPU: VDDA25



C --> CORE 1V05

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F --> XCVR Clk Ref 10k

B --> XCVR Clk Buf 2V5

P --> XCVR PLL 2V5

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10 Layer Stackup Study for the DK PCB

Current Rev. 4-Oct-2023

Study to see if DK can be routed on a balanced 10 Layer design.

Layer	Function	Copper Weight
1	Traces and Pads	1/2 oz
2	Gnd Plane	1/2 oz
3	Traces & Power Fills	1/2 oz
4	Gnd Plane	1/2 oz
5	Power Fills	1 oz
6	Power Fills	1 oz
7	Gnd Plane	1/2 oz
8	Traces	1/2 oz
9	Gnd Plane	1/2 oz
10	Traces and Pads	1/2 oz

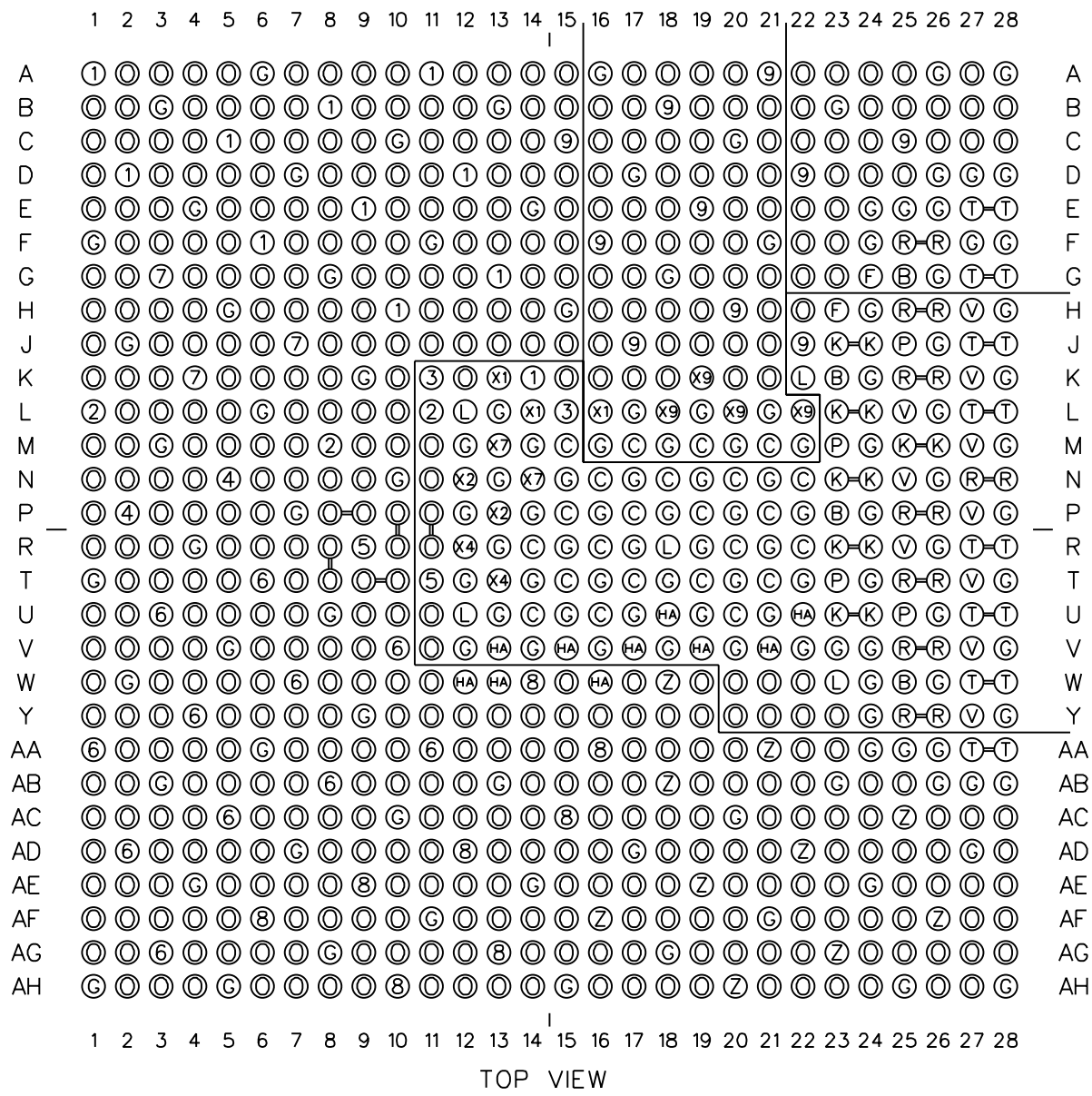
All trace layers (1, 3, 8, 10) must be able to support 76 & 100 Ohm differential trace pairs and 40 & 50 Ohm single ended routes.

- The Zo of the differential pairs should come from a 50/50 balance of Ground Reference and opposite side reference.
- An approximate velocity match of the single ended microstrip and stripline is a big advantage.

All power routing will be done with fills on layers 3, 5, and 6. No power layer can be dedicated to a single rail.

Physical Layer: 3

DIGITAL_2V5 and FPGA_PLL_2V5



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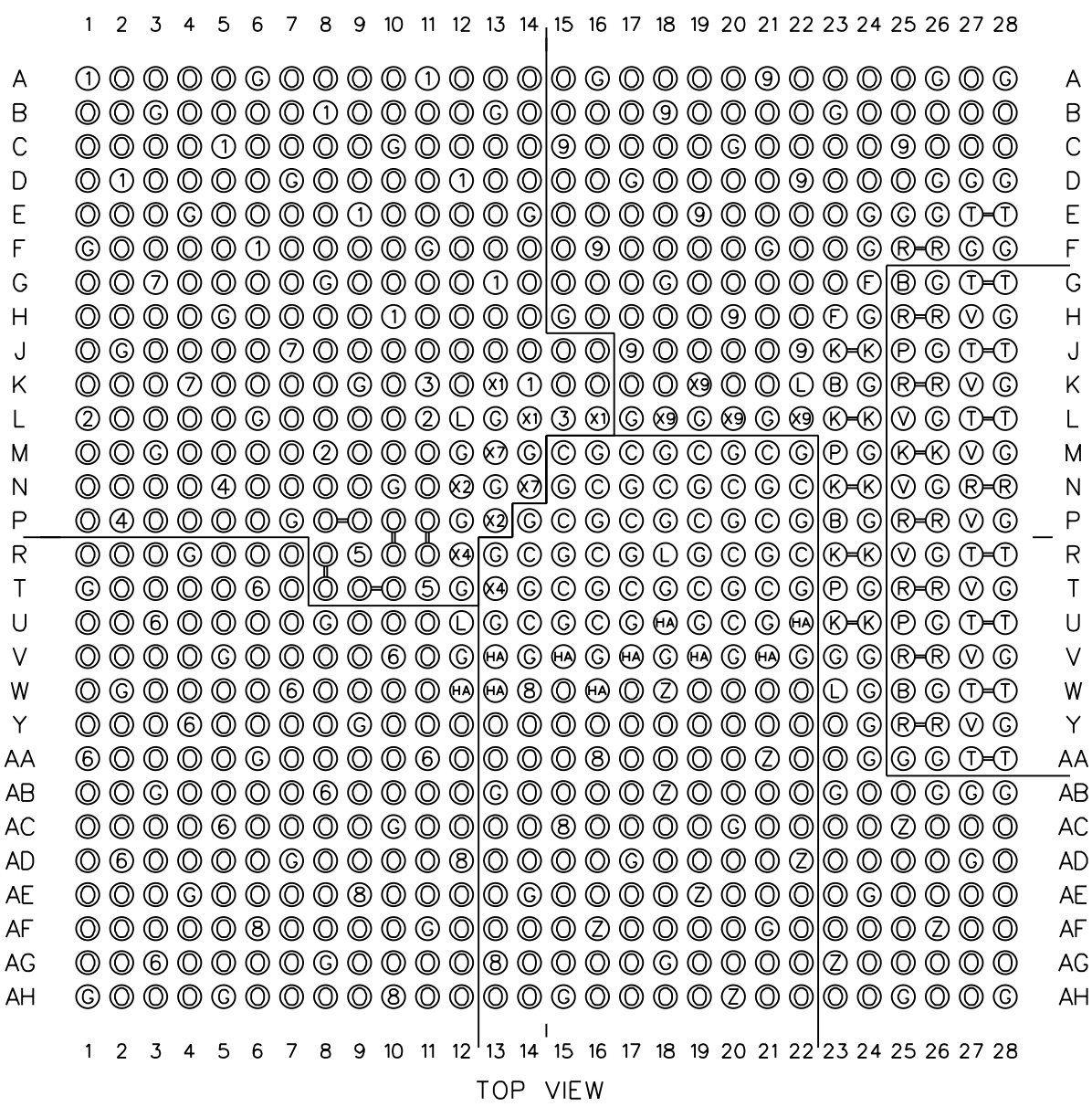
DK Planes Drw. 12 Rev. 11-Sept-2023

Physical Layer: 5

BULK_3V3 and CORE_1V05 and XCVR_1V05



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K --> XCVR Clk Input

Z --> Bank 0 VDD

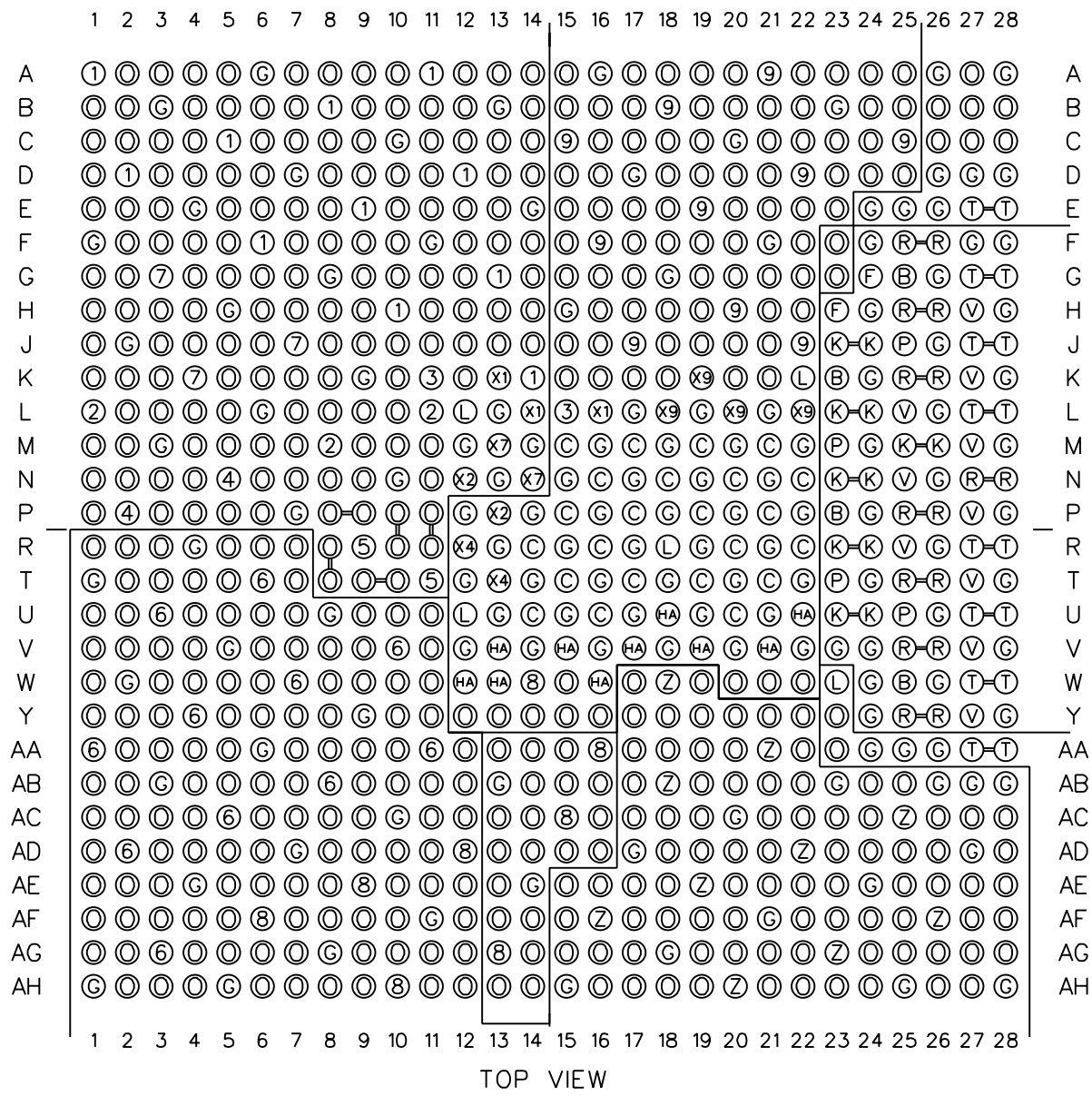
1:9 --> Banks 1:9 VDD

1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD

DK Planes Drw. 10 Rev. 11-Sept-2023

Physical Layer: 6

DIGITAL_1V8 and BULK_1V2 and XCVR_CLK - XCVR_PLL



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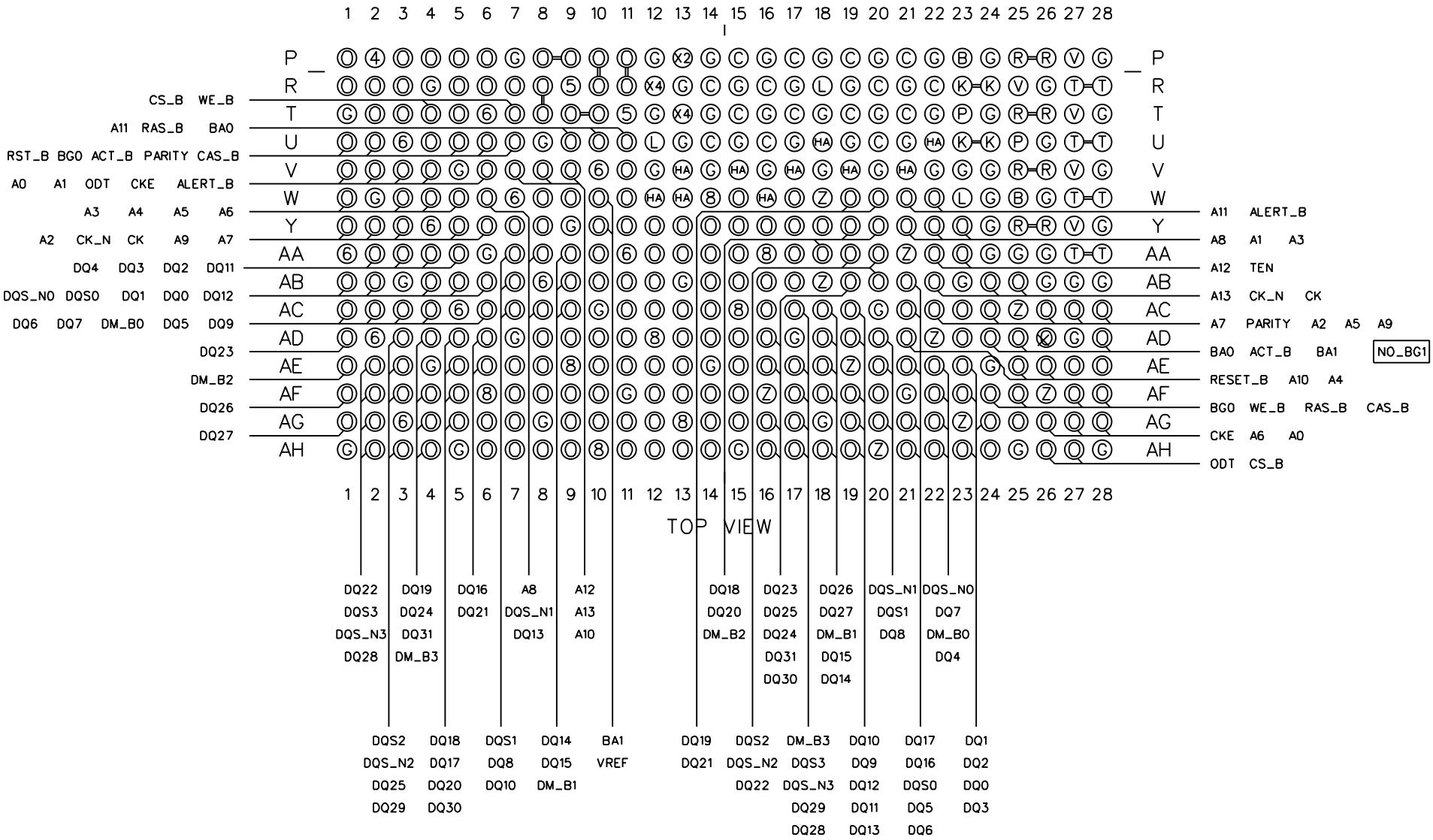
DK Planes Drw. 11 Rev. 11-Sept-2023

DDR4 Escapes from Banks: 0, 6



DK Planes Drw. 13

Rev. 13-Sept-2023

Viasystems Technologies Corp. LLC
8150 Sheppard Ave E
Toronto, ON, M1B 5K2

Job Name : 181875
Customer : DEBRON INDUSTRIAL ELECTRONICS
Part Num : 40-00643-00LF
Part Rev : -
Engineer : Yogi Perin

Layer	Cust Thickness	Calc Thickness	Primary Stack	Description	Dk / Df
		0.0005		Taiyo 4000-HFX DI	3.50 / 0.0190
Layer - 1		0.0020		**1/2oz Mix (Std Plt)**	
		0.0038	1080 - 71%	FR408HR	3.42 / 0.0098
Layer - 2		0.0006		**1/2oz P/G**	
		0.0100	0.0100 (2-2116)	FR408HR	3.69 / 0.0089
Layer - 3		0.0006		**1/2oz Sig**	
		0.0040	3313 - 63%	FR408HR	3.48 / 0.0096
Layer - 4		0.0006		**1/2oz P/G**	
		0.0180	0.018 (3-1652)	FR408HR	3.90 / 0.0083
Layer - 5		0.0012		**1oz Mix**	
		0.0078	2116 - 55% 2113 - 57%	FR408HR	3.64 / 0.0091
Layer - 6		0.0012		**1oz Mix**	
		0.0180	0.018 (3-1652)	FR408HR	3.90 / 0.0083
Layer - 7		0.0006		**1/2oz P/G**	
		0.0040	3313 - 63%	FR408HR	3.48 / 0.0096
Layer - 8		0.0006		**1/2oz Sig**	
		0.0100	0.0100 (2-2116)	FR408HR	3.69 / 0.0089
Layer - 9		0.0006		**1/2oz P/G**	
		0.0038	1080 - 71%	FR408HR	3.42 / 0.0098
Layer - 10		0.0020		**1/2oz Mix (Std Plt)**	
		0.0005		Taiyo 4000-HFX DI	3.50 / 0.0190

Materials: Isola FR408HR High Speed High-Tg FR4

Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0940	0.0094	0.0094	0.0904
Incl. Mask over Laminate	0.0900	0.0090	0.0090	0.0864
Incl. Plating	0.0930	0.0093	0.0093	0.0894
After Lamination	0.0902	0.0045	0.0045	0.0866
Over Laminate	0.0890	0.0089	0.0089	0.0854

Note

IPC-6012 has a minimum dielectric requirement of .003543" and any nominal dielectric .0045" or less may violate this requirement based on vendor tolerances and actual lamination yields. Accepting TTM`s stackup will be taken as a waiver against this requirement. With this exception, minimum dielectric thickness shall be .000984". If this is not acceptable please advise immediately so options can be reviewed and discussed. If we do not get a response within 24 hours, we will proceed with this stackup. Please also be advised that accepting this stackup has no impact on TTM meeting IPC-6012 Class 2 or Class 3 requirements. Please also note that nominal targeted dielectric gaps of .0046" or greater shall have a minimum tolerance of +- .001" after lamination.

Job Comment

6 different back drills required.

Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
1 EC Microstrip	L1	0.00550	0.0055	0.0157	-	100	10	101.98
	-	0.00550	0.0055	-	L2			

Viasystems Technologies Corp. LLC
8150 Sheppard Ave E
Toronto, ON, M1B 5K2

Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
2  EC Stripline	L3	0.00550	0.0053	0.0157	L2	100	10	100.85
	-	0.00550	0.0053	-	L4			
3  EC Stripline	L8	0.00550	0.0053	0.0157	L7	100	10	100.85
	-	0.00550	0.0053	-	L9			
4  EC Microstrip	L10	0.00550	0.0055	0.0157	L9	100	10	101.98
	-	0.00550	0.0055	-	-			