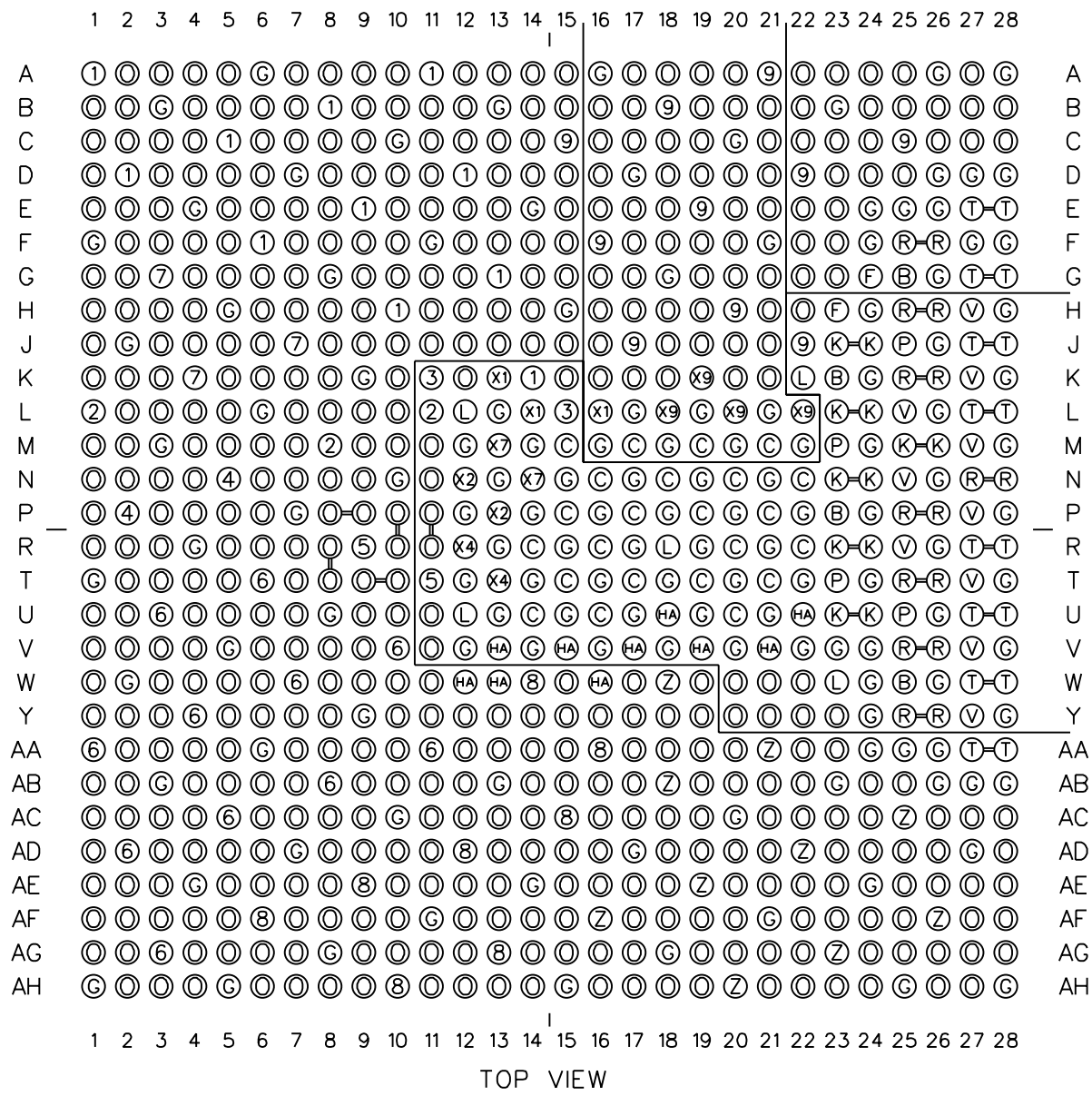
Physical Layer: 3

DIGITAL_2V5 and FPGA_PLL_2V5



C --> CORE 1V05

L --> PLL & PNVM 2V5

HA --> PROG & HSIO Aux 1V8

F --> XCVR Clk Ref 10k

B --> XCVR Clk Buf 2V5

P --> XCVR PLL 2V5

V --> XCVR Tx&Rx 1V05

T --> XCVR Tx Output

R --> XCVR Rx Input

K --> XCVR Clk Input

Z --> Bank 0 VDD

1:9 --> Banks 1:9 VDD

1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD

DK Planes Drw. 12 Rev. 11-Sept-2023