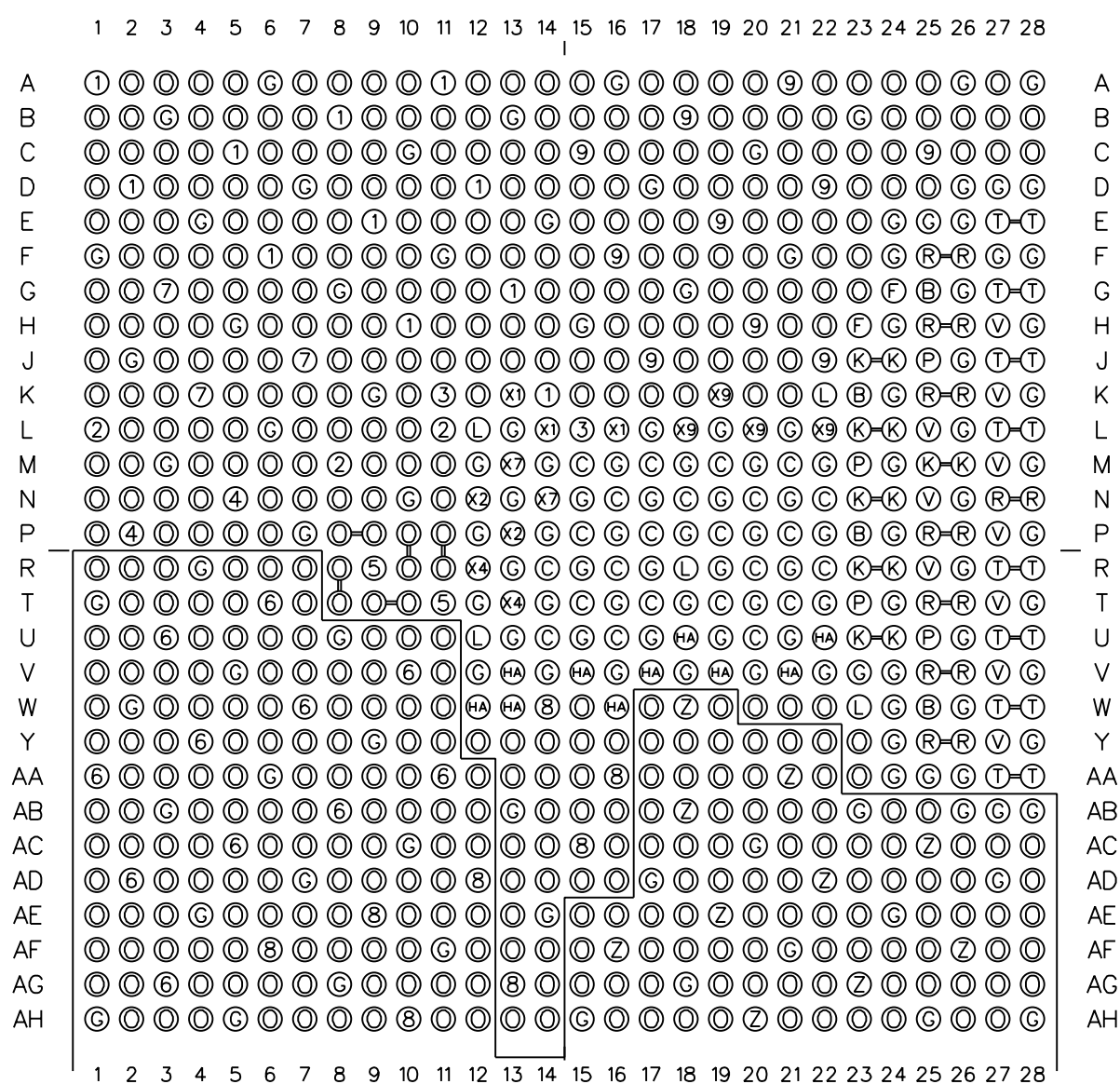


# DK Board - FPGA/CPU - Minimum BULK\_1V2 Plane

## BULK\_1V2 Connects to: I/O Banks 0 & 6 and DDR4 Memories



TOP VIEW

- C --> CORE 1V05
- L --> PLL & PNVM 2V5
- HA --> PROG & HSIO Aux 1V8
- F --> XCVR Clk Ref 10k
- B --> XCVR Clk Buf 2V5
- P --> XCVR PLL 2V5
- V --> XCVR Tx&Rx 1V05
- T --> XCVR Tx Output
- R --> XCVR Rx Input
- K --> XCVR Clk Input
- Z --> Bank 0 VDD
- 1:9 --> Banks 1:9 VDD
- 1x, 2x, 4x, 7x, 9x --> Banks 1,2,4,7,9 AUX VDD