Speaking Notes DK Review 10-Oct-2023

Rev. Date: 9-Oct-2023

- Can not show you a detailed completed design but can show you where we are in our thinking about the DK design and something about our design process.

- Eventually will need a detailed review.

- These are drawings to help people Understand the design of the various functions. These are not the engineering schematics to Implement the design.

- About 60 slides and too little time --> very brief comments - just to give you an idea of what each drawing is about.

- URL for the DK web pages at MSU - about 1000 files available:
  Comp Types Lists (part types vs pick-place) GPIO Signal List

DK Circuit Diagrams:

pdf page	Drw Num	
2	46	EPON Timing Distribution version of the Block Diag No details, major blocks only Balance of details vs readability
3	1	PS Overall - For reliability minimize count --> Analog and Digital All DC/DC is done with modules for switching noise Auxiliary PSs DDR and Always On are not shown Provides power to DK loads and to non-DK loads
4	2	100V -> 5V - Need for Input Filter: Noise on Cable & Stiff 100V Feed to Final Test Monitor Test Connector - No probing Always ON when input power is available No Aluminum Electrolytics --> large Polypropylene
5	3	5V -> POL - Up on Module PCB to control circulating current noise TI Mods - Used before - MTBF Specified Input Current Monitor Input noise filter to keep from passing noise around Ramp up on a Volt per Volt basis UVLO for shutdown Trim because temp & life better than initial calibration Sense before LC output filter - Low R Chokes LC filter factor of 300 under Switching Frequency Zener Clamp (can not clamp supply - last cycle) Output Voltage Monitor to PS Monitor Connector
6	6	DDR Term & Ref - Separate supplies for CPU and FPGA DDR Memory Type that Tracks the 1V2 Mem power - As Recommend

7	7	Always-ON 3V3 - Is ON anytime there is 5V power available Runs a small amount of Supervisory Power Up Logic.
8	45	FPGA/CPU Feeds - 22 feeds to the FPGA/CPU - Can be confusing Lists under Function - 2x I/O Blk - See again later
9	9	PS Startup - Satisfy start up requirements of all power consumers Minimize Spikes on Source - Ramp Volt per Volt bases Slow - No need for speed Allow Quartz Osc to stabilize before Reset is Released Whole String cold start will be a slow process
10	4	Start Super - Releases the Track Bus after 1 sec of cont stable 5V
11	5	All Pow Good - Release the Resets after 1 sec of cont stable 3V3 Initial more complicated scheme - verify each PS If any one PS goes Down --> Module is Down General principle - keep it simple & Fully Understood No in place readback - because can not Access Fix Simple & Reliable is Best
12	55	Resets #1 - Lock some things out until CPU is Awake & Sane Unknown State of IOs during some parts of cold start Set things up - then assert Sane Discrete Logic
13	56	Resets #2 - More of same Will see more use of CPU Sane in ER
14	49	I2C Buses - Separate by Access - DAQ vs Specialized Control
15	48	SPI Buses - BOOT Memories - FPGA BOOT is Main One - more later Interposer - more later
16	59	CPU Boot Mem - of secondary importance
17	12	FPGA Boot Mem - This Boot Must work - ER Connection - more later Emergency Rescue can overwrite this boot memory
18	13	JTAG Conn - Used Only for Testing and initial power up - Buffer isolation - no zap if casually plugged in
19	60	UART List - CPU and Emergency Rescue
20	14	Clocks #1 - CPU and Spare - CPU Osc actually for multiple things
21	64	All Clocks - CPU, XCVR Enet Ref, FPGA, Monitor Monitors to prove design and test each card - Must Work No probing - Long test runs may be useful Serious Experiment Synchronous Clk to ADC and FPGA Spare - Connected to Best Possible Inputs Various Choices - Power Limitation
22	54	Clk to Other - Minimize use of Low Q little crystals - fewer parts
23	22	PMT ADC Pow - 4x power feeds - All filtered Separate 1V0 - same Bulk 1V8 but 2x LC Filters Does consume power - Si Temp Diode next page
24	16	PMT ADC Signals - SPI and other slow controls from FPGA/CPU

Clocks are direct from the Timing Generator
4x Serial output - 12.7 Gbps per lane

25 10 PMT ADC PMT Analog Input - ADC Input is Bipolar & Differential
Need DC Offset to 80 % of negative FS
Flat frequency response:
0.4 MHz - 200 Mhz 3 dB
0.5 100 2 dB
5.0 80 1 dB
50 Ohm Termination in this Band
A Main Concern: 0.2 mV per LSB
Ground Loops that include Switching
Power Supplies -> we will have Noise
Can operate Pseudo Differential
Input if that is best
About 10 parameters setup in ADC Registers
that control how the ADC works and
parameters are common to all 16 Channels.

26 62 PMT ADC Photo-Diode Analog Input - 1.62 V FS 200 Ohm
Back Terminated at the source
Much lower input Frequency
under 1 MHz
PCB must be able to do either
with no compromize to PMT

27 17 USB #1 - Connection to USB Phy Chip from dedicated FPGA/CPU pins
The Reset powers down the Phy Chip and USB Load

28 18 USB #2 - Power Control with I Limit and Fuse - Use of Fuses

29 23 Timing Generator - Power Feeds - may move to all 1V8
Setup and Control from the private I2C link to
reduce risk of corruption during norm operation

30 50 Timing Generator - Shows the Input and Output timing signals
Auxiliary Inputs for TDC signals because
this Timing Gen can provide TDC function.

31 51 SPI to Interposers - 1 Controller 2 Buffered Conn to Interposers
2x SPI CS select the target Interposer
3x GPIO Adrs lines select the target on
the selected Interposer

32 52 Other Conns to Interposers - Separate 40 pin Conn for each
Interposer
Pinout is in the Connectors file
on the web - one runs backwards
Flash Now single End or LVDS - TDC
Ctrl Reset - Muon FPGA TDCs
UARTs separate for Inter 1 and 2
Filtered Power No Fuses - Diff Piezo

33 36 Envron Sensor - I think these are the same parts as used before
Required post assembly processing
Strange pinout - I’m verifying

34 37 BB Audio ADC - Setup & Ctrl via I2C at 100 kHz max
Clock from FPGA - Can adjust - Data to FPGA
AC coupled input - Can set low Frequency

2 spare inputs - this is a fancy quality ADC

35	38	FPGA Memory	- 4 GBytes 32 bit wide data path Must Work
36	39	CPU Memory	- 4 GBytes 32 bit wide data path Both use the same Single Rank Memory Design Both are non-ECC memories systems Not LPDDR4 completely different specification and not of use in this application DDR4 800 MHz 32 bit transfer every 0.625 nsec In the FPGA/CPU the FPGA & CPU Memory Controllers are different. Poor Documentation & we still have many questions In general they say - Design Tool is top Authority Which features work on which Memory Controller Command Adrs Bus - Parity protection Pinout Options - useless Guard Pins - Talk but demo makes limited use TEN Test Enable Built in CRC - but what about Controller use Post Package Spare Row Replacement learn how Which features are in use is setup by Registers in the Memory Chips - Datasheet 370 pages Using Internal Ref in FPGA/CPU Controllers and a 1V2 tracking Ref in each memory array FPGA/CPU Memory Controllers do not have an easy to use pinout but the immediately adjacent pin fields are clear for under chip bypass & Gnds. More points later in the PCB description files.
37	42	SFP Conn and Cage	- Connections shown Ethernet to FPGA/CPU If EPON Timing then SANE supervision of the Laser ON control. Chicken - Egg for Boot
38	53	HS XCVR Usage	- Only Ethernet RxTx and PMT ADC Data 4x Rx Sparse usage of HS XCVR pin field - Good
39	43	Barnacle Connector	- Power, Reset, Clocks, UART Data, GNDs Reset should turn OFF all power usage
40	44	Emergency Rescue	- Can over write the FPGA’s Boot PROM RS-485 Half Duplex Comm --> Offset Terminator ER_SANE protect Boot PROM take over and RS-485 Transmit Enable ER uProc Code - simple: Hello/Ping, Term, PROM ER uProc has built in unique Serial Number
41	47	Emergency Rescue	- Power connection & Std ARM DeBug Connector

DK PCB Design:

- 1400 PCBs so must control the cost: layer count & required technology

- Need High quality bare boards for high quality assembly & long life

- Laminate Types, dielectric layer thicknesses, trace widths - Zo control,
  via aspect ratio, mechanical strength,

- Effective Panalization in bare board manufacture for cost control

- Controlled Zo:

    Microstrip & Stripline Differential pair 76 & 100 Ohm
    Microstrip & Stripline Single Ended 39 and 50 Ohm

    Microstrip on Outer Layers   Stripline on Inner Layers

pdf page	Drw Num		
2	26	Brd Size and Circle	- Probably have Seen this slide before
3	63	Brd Floor Plan	- Size and arrangement based on routing sketches Arrangement of DC/DC will make sense - spokes
4	25	FPGA/CPU Pin Field	- No drawing in documentation
5	61	FPGA/CPU BANKS	- Run through Mem, GPIO, HS XCVR
6	45	FPGA/CPU Power Feeds	- 22 feeds must be by power fills How many PCB Physical Layers will be Required for the Power Fills ? FPCA/CPU power feeds and Memory system routing are the driving factors for pcb layer count.
		Minimum Power Fills for FPGA/CPU 9 Required	
7	6	Bulk_1V2 to	Banks: 0 & 6
8	1	Bulk_3V3 to	Banks: 1, 2, 3, 5, 7
9	5	CORE_1V05 to	Core
10	2	Digital_1V8 to	VDD18 and Bank 9
11	3	Digital_2V5 to	Bank 9 Aux
12	4	FPGA_PLL_2V5 to	VDD2V5
13	7	XCVR_1V05 to	VDDA
14	9	XCVR_CLK_2V5 to	XCVR_CLK
15	8	XCVR_PLL_2V5 to	VDDA25
16		Text of 10 layer Stack Study	- 4 Routing Layers Minimum required for Memory - 3rd Layer power fills not allowed under Memory - Length Match for Memory Cmd-Adrs & 2x Data - Via Match for Memory - uStrip vs Stripline Match for Memory - pcb adj - Plugged Thermal Vias on Top side - No Back Drill for HS - single transition to L6
17	12	Physical Lay 3	- Digital_2V5 & FPGA_PLL_2V5 Low Current Quiet 0.5 oz copper, can not be under Memory Banks
18	10	Physical Lay 5	- Bulk_3V3, Core_1V05, XCVR_1V05
19	11	Physical Lay 3	- Digital_1V8, Bulk_1V2, XCVR: Clk & PLL
20	13	Escapes for DDR Memory Study	- This is the highest concentration of BGA Escapes and Deepest Rings Other escapes should be OK Layout Not good but OK

No proof can achieve the required signal order and have space for Serpentine Length Matching 0.5 mm

Example 10 Layer Stackup from a previous build with HS signals