Disko-Kraken
Circuit Board
Hardware Design

- Overview, Goals and Concerns
- Hardware Functions on the DK Board
- My view of DK Milestones

DK Board: Overview, Goals and Concerns

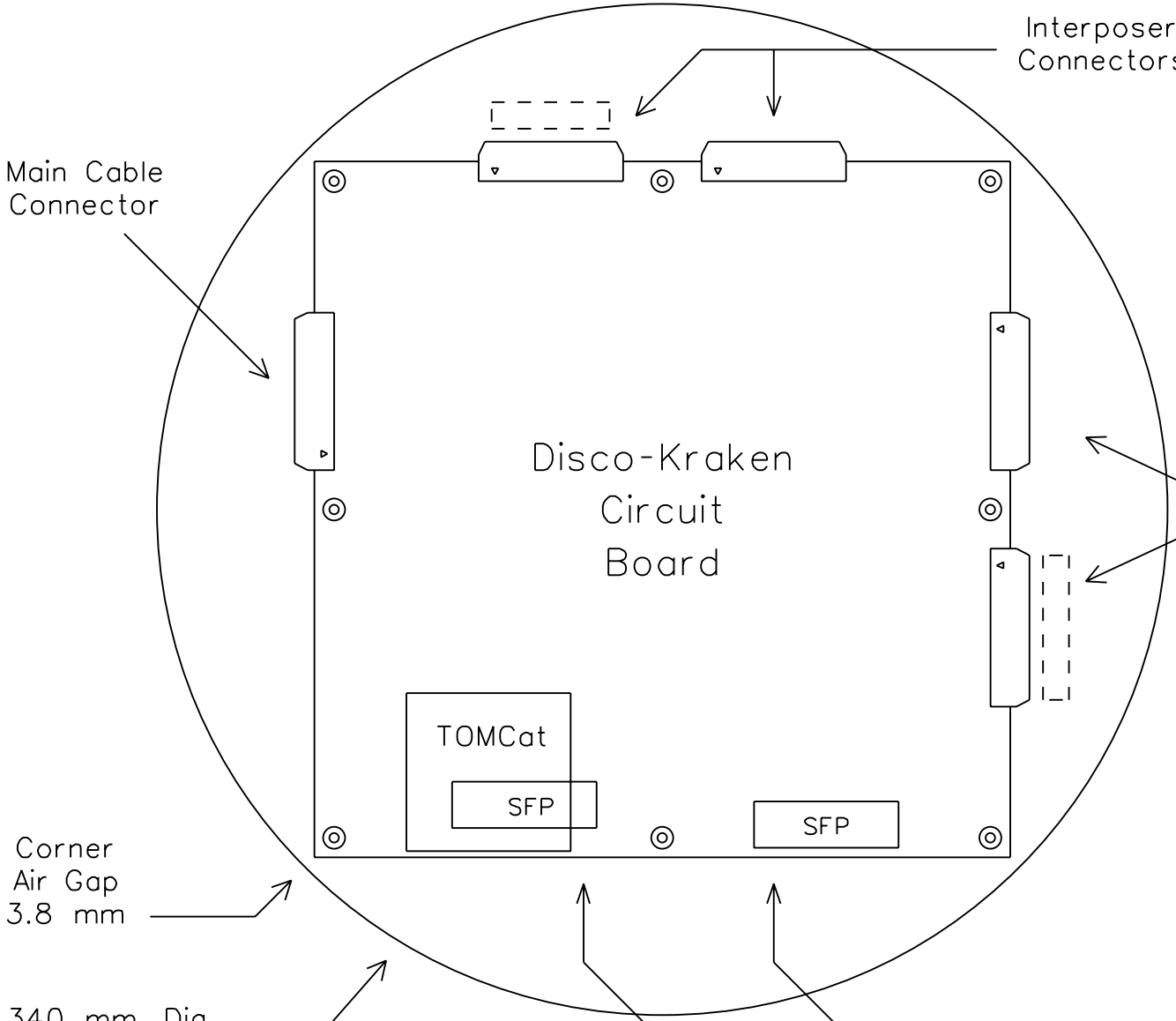
Overview:

- Physical Size - see page 3
- Location of Connectors
- Required Cable Pass-Through Holes in the Mounting Plate
- Designed to facilitate final assembly

Goals and Concerns:

- Would like the prototype of the DK board to be as close to the Final Design as possible - minimize the risk when going from prototype build to production build - minimize any difference in Physics performance or analysis between revisions
- Cost Control - we need 1400 of these circuit boards - do not use unnecessary fancy or expensive technology - control the PCB layer count and eliminate manufacturing steps where possible

Disco-Kraken - Board Size and Layout



DK Board Size:
235 mm Square

Vertical Space Available: 30 mm

4.0 mm Under PCB
2.5 mm PCB Thickness
22.5 mm Max Comp Height
1 mm Air Gap Above Max Comp

PMT Signal Connectors

Holes in the Mounting Plate for Cable Pass Through

Mounting Screws

DK Board: Goals and Concerns Continued

- Design for a high Manufacturing Yield - use conservative design rules where ever possible - follow IPC guidelines - visit the assembly house to understand their concerns
- Designed for Reliability and Long Life - follow guidelines for reliable long life electronics - use common sense about component selection, e.g. no aluminum electrolytic capacitors
- Design for Low Power - this has not been a common concern for our previous work - must pay attention to this
- The design must facilitate Final Assembly and Testing - need to understand the long term plans in this area
- Too many Sole Source Parts - this situation is exacerbated by the manufacturing schedule being spread over years - this is an issue for management attention
- Need to understand more about the environment inside the module - heat, humidity, mechanical shock
- Noise in the PMT Signals or in their ADC - we need the full 12 bit dynamic range and 5 nsec sampling to do the Physics - issues of ground loops and tight space so limited isolation

Hardware Functions on the DK Board:

1. Power Supply Section - 100 VDC Input Power - Outputs:
   - 5V0, 3V3, 2V5, 1V8, 1V2, 1V05, 1V0_Core, 1V0_ADC, 0V6
   - 5V0, 3V3, 1V8 are supplied to: TOMCat and Interposer
   - Power Supply Startup Ramp Rate is controlled to meet the requirements of all ICs
   - Power Supply Startup includes control of the Rest signal to: FPGA/CPU, PMT ADC, Clock Generator, Ethernet, and Bluetooth
   - Power Supply Section includes control of the power feed to: TOMCat, Bluetooth, Ethernet, Inductive Power Coupling, and to parts of the Clock Generator, no control of Interposer power
2. FPGA/CPU Section:
   - 4 GBytes of memory for the FPGA - used for a Buffer for the PMT ADC Data
   - 4 GBytes of memory for the CPU - used for Linux and for the application programs that operate the module and for data
   - Separate Non-Volatile Boot Configuration Memories for the FPGA and for the CPU

Hardware Functions on the DK Board:

3. ADCs for 16 PMT Signals - 12 bit resolution - sample every 5 nsec
4. Support for the TOMCat which provides 125 MHz and 1 Hz time base and 1 Gbps Ethernet Communication to the DK board
5. Clock Generation: PMT ADC Clock and the Flash-Now signal are based on the TOMCat reference, other clocks are provided to: FPGA, CPU, Ethernet, TDC, USB, Bluetooth, and Audio ADC
6. Ethernet communication 1 Gbps via TOMCat to shore
7. Ethernet communication 10 Mbps up/down Main Cable to adjacent modules
8. Timing Signals up/down Main Cable to adjacent Modules
9. Interposer connections and device support:
   - Power supplied to the Interposer
   - SPI and UART Interposer communications with 3 address lines
   - Hydrophone signal from Interposer to audio ADC
   - 4x Muon signals from Interposer to FPGA I/O
   - Flash-Now timing signal from DK's Clock Generator to Interposer
   - Light-Seen signal from Interposer to TDC

Hardware Functions on the DK Board:

10. Accelerometer and Magnetometer sensors for the module's position determination
11. USB connection for the module's Camera
12. Bluetooth and Inductive Power Coupling for the module's External Sensors
13. Support for the Emergency Rescue RS-485 connection
14. Access Connections - for the Initial Testing and then for Production Testing of the DK boards:
    - Connector for JTAG to FPGA and CPU
    - Connector for Power Supply Voltage and Current tests
    - Connector for "Access Signals": Clocks, FPGA/CPU I/O

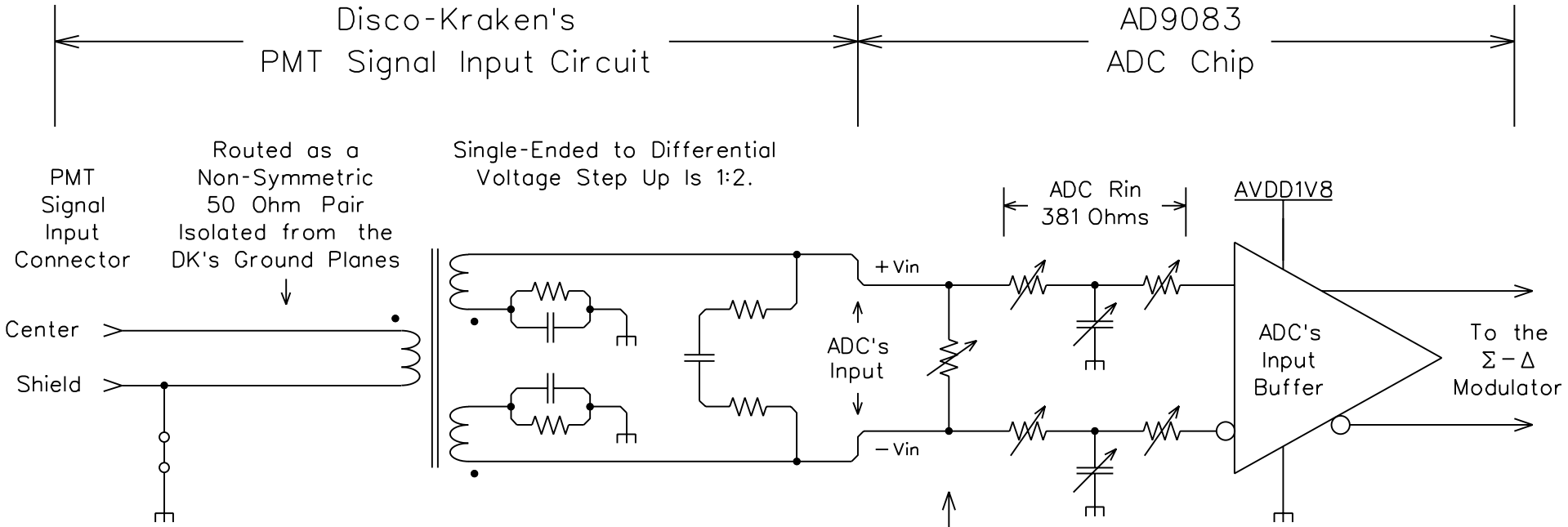
Milestones to a Useful DK Board:

- The requirements for DK are stable.
- The design of DK is fully described in detailed documents and drawings all of which are available on the web for review.
- Design of the DK PCB is finished - all files for the manufacture of the bare PCB and for the assembly of the boards are ready for review and then release. A vendor for all DK builds has been selected and a PO is in place.
- Delta time for the actual build of the cards.
- Initial hardware only tests, e.g. are the power supplies OK, are all clocks running, does JTAG work, no visible smoke
- "Private" development work at MSU of Firmware and Software along with continued testing of the hardware itself, e.g. make a detailed evaluation of the PMT ADC's performance.
- DK is ready for tests outside of MSU, e.g. integration tests with TOMCat and the Interposer.

  Need to support stand alone operation of DK outside of MSU.

  Focused on the DK functions that must work at Rev A.

PMT to ADC Input Analog Circuit



DC Bias Set to 80% of Negative Full Scale.

Overall Parallel AC Termination Is 200 Ohms.

See Datasheet
Pages: 5 note 6,
30, and 31.

For the ADC's Input to Swing from Its Static 80% of Neg. FS to 100% of Pos. FS Requires a 0.81 V Pulse Across the Primary of the Transformer aka 16.2 mA through 50 Ohms.

The Capacitor Symbol
Represents Parallel
1 uFd and 47 nFd
Ceramic Capacitors

The Recommended
Common Mode at
the ADC's Input
is 0.7 Volts

The ADC's Nominal
Vmax is 1.8 Vpp
---> Pos. Full Scale Is:
+Vin 1.15V −Vin 0.25V
---> Neg. Full Scale Is:
+Vin 0.25V −Vin 1.15V

The ADC
Actively Holds
the Inputs of Its
Input Buffer at a
Common Mode
of 1.1 Volts

DK Drw. 10
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