H-Clk FPGA Global Clock Receivers and 40 MHz PLL Pre-Scaler

10 MHz GPS Clock PLL Reference Clock

To Any Other Uses of the 10 MHz Clock in the H-Clk FPGA on a Global Clock Net

Reference to the PLL's Phase Comparator

FPGA's LVDS Driver

FPGA's LVDS Receiver and Global Clock Buffer

40 MHz PLL Logic Within the H-Clk FPGA

To All Other Uses of the 40 MHz Clock in the H-Clk FPGA on a Global Clock Net

Divide by 4

Feedback to the PLL's Phase Comparator

1 PPS GPS Signal

To the User's of the 1PPS Signal within the H-Clk FPGA

Revision: 1-DEC-2011