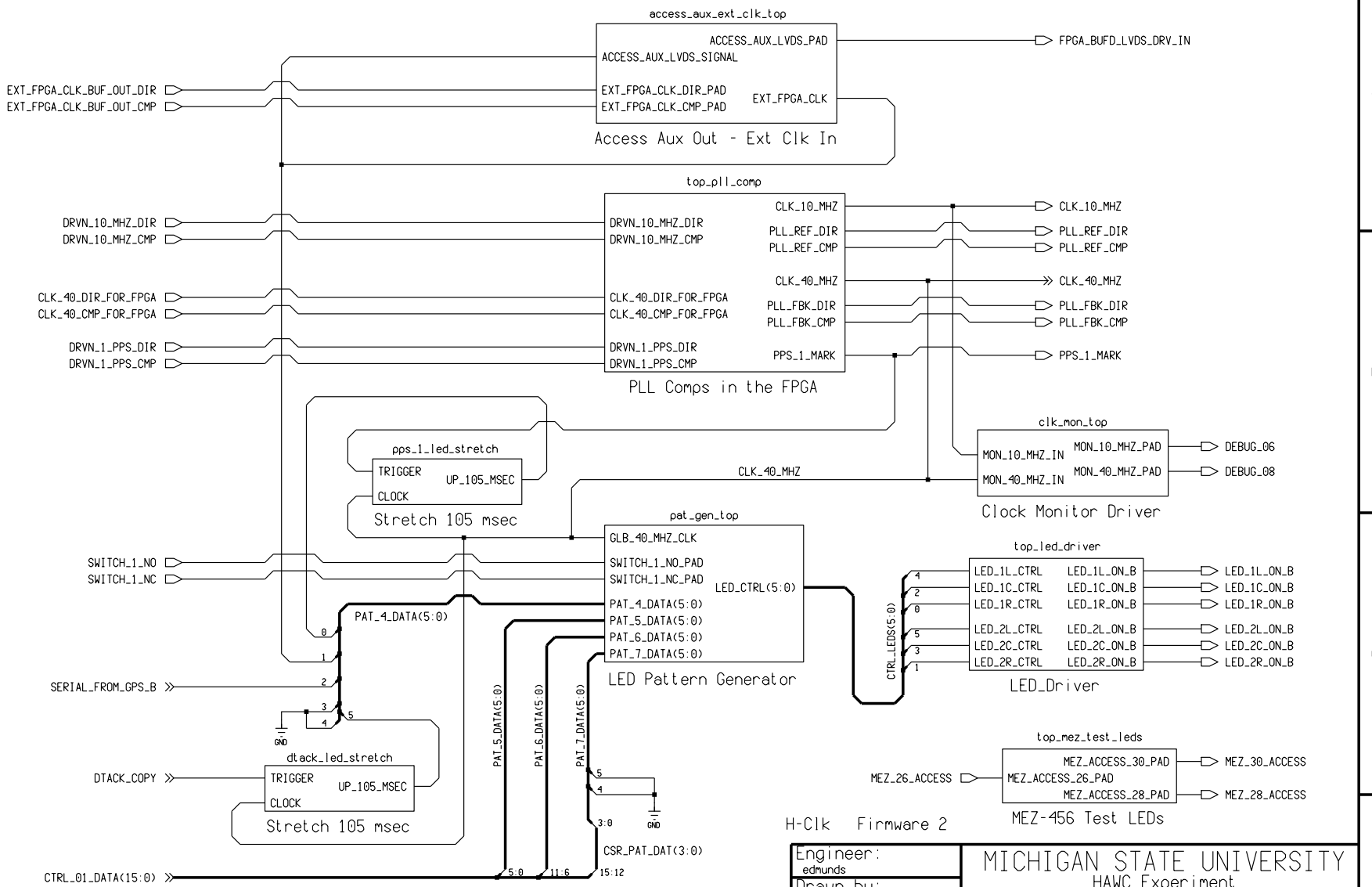
access_aux_ext_clk_top
ACCESS_AUX_LVDS_PAD
ACCESS_AUX_LVDS_SIGNAL
EXT_FPGA_CLK_DIR_PAD
EXT_FPGA_CLK_CMP_PAD
EXT_FPGA_CLK
FPGA_BUFD_LVDS_DRV_IN
EXT_FPGA_CLK_BUF_OUT_DIR
EXT_FPGA_CLK_BUF_OUT_CMP
Access Aux Out - Ext Clk In
top_pll_comp
DRVN_10_MHZ_DIR
DRVN_10_MHZ_CMP
CLK_40_DIR_FOR_FPGA
CLK_40_CMP_FOR_FPGA
DRVN_1_PPS_DIR
DRVN_1_PPS_CMP
CLK_10_MHZ
PLL_REF_DIR
PLL_REF_CMP
CLK_40_MHZ
PLL_FBK_DIR
PLL_FBK_CMP
PPS_1_MARK
PLL Comps in the FPGA
pps_1_led_stretch
TRIGGER
UP_105_MSEC
CLOCK
Stretch 105 msec
clk_mon_top
MON_10_MHZ_IN
MON_40_MHZ_IN
MON_10_MHZ_PAD
MON_40_MHZ_PAD
DEBUG_06
DEBUG_08
Clock Monitor Driver
pat_gen_top
GLB_40_MHZ_CLK
SWITCH_1_NO_PAD
SWITCH_1_NC_PAD
PAT_4_DATA(5:0)
PAT_5_DATA(5:0)
PAT_6_DATA(5:0)
PAT_7_DATA(5:0)
LED_CTRL(5:0)
LED Pattern Generator
top_led_driver
LED_1L_CTRL
LED_1C_CTRL
LED_1R_CTRL
LED_2L_CTRL
LED_2C_CTRL
LED_2R_CTRL
LED_1L_ON_B
LED_1C_ON_B
LED_1R_ON_B
LED_2L_ON_B
LED_2C_ON_B
LED_2R_ON_B
CTRL_LEDS(5:0)
LED_Driver
SWITCH_1_NO
SWITCH_1_NC
SERIAL_FROM_GPS_B
GND
dtack_led_stretch
DTACK_COPY
Stretch 105 msec
top_mez_test_leds
MEZ_ACCESS_30_PAD
MEZ_ACCESS_26_PAD
MEZ_ACCESS_28_PAD
MEZ_26_ACCESS
MEZ_30_ACCESS
MEZ_28_ACCESS
MEZ-456 Test LEDs
CSR_PAT_DAT(3:0)
CTRL_01_DATA(15:0)
H-Clk Firmware 2
Sheet 2 contains the 10 GPIO connectors
Sheet 3 is the VME I/F and Serial I/O
Engineer: edmunds
Drawn by: --
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:
MICHIGAN STATE UNIVERSITY
HAWC Experiment
H-Clk Firmware 2
TITLE:
HAWC H-Clk Firmware
H-FIRM-2 Top Sheet
Sheet 1 of 3
Size: C
Changed by: edmunds
Date Changed: Sunday 5-MAR-2012
Time Changed: 12:00:00
QA CHK:
REV:
Drawing Number:
Page: 1