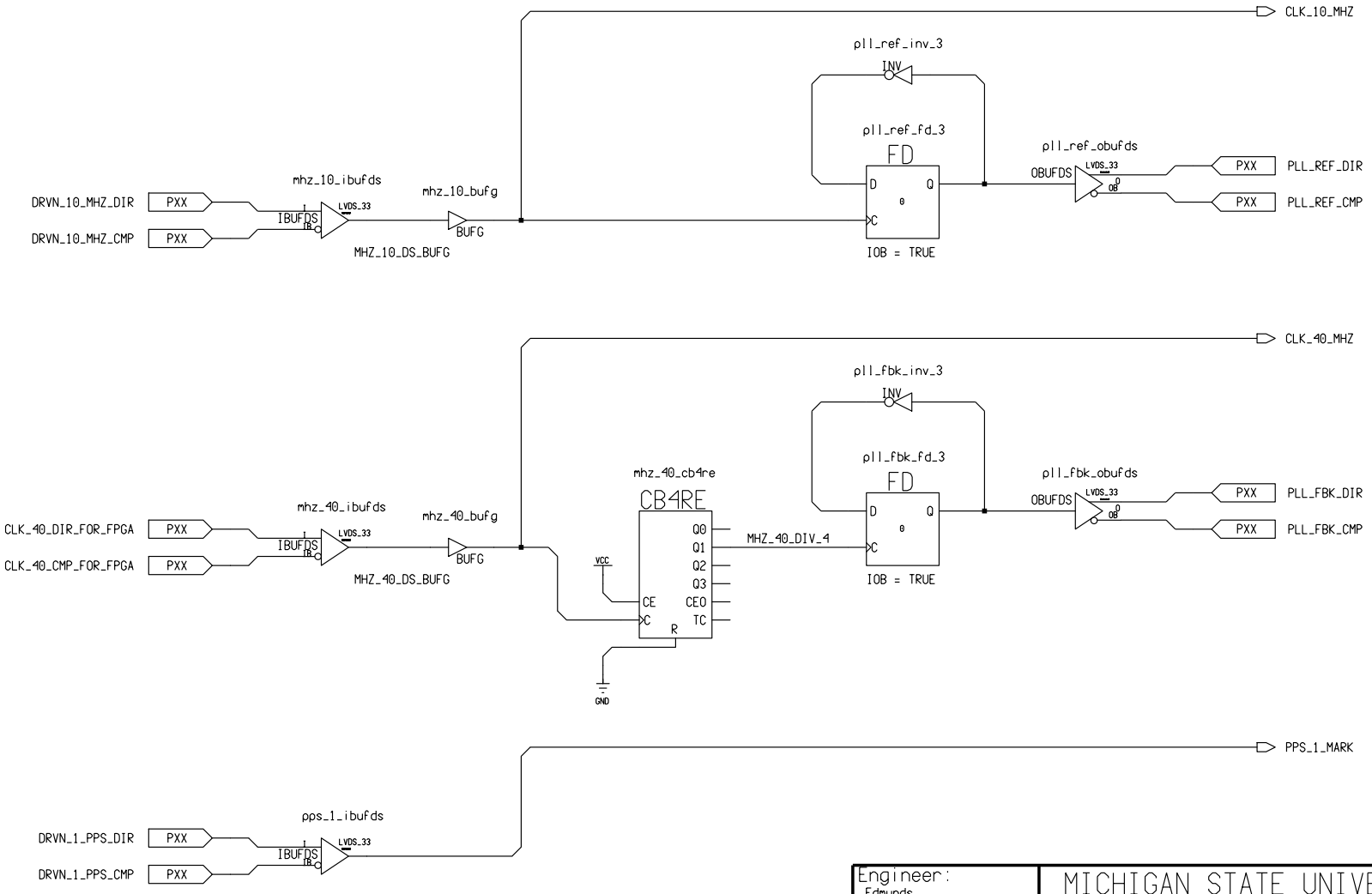

This sheet is the 40 MHz PLL components that are in the FPGA.

This includes the 10 MHz and 40 MHz Global Clock Receivers.

Engineer: Edmunds	MICHIGAN STATE UNIVERSITY HAWC Experiment H-Clk Firmware 1
Drawn by: Librarian	
R&D CHK:	TITLE: HAWC H-Clk Firmware 1 40 MHz PLL Components in FPGA Sheet 1 of 1
DOC CTRL CHK:	Size: C
MFG ENGR CHK:	4144
Changed by: Edmunds	Date Changed: Sunday 12-FEB-2012
Time Changed: 12:00:00	QA CHK:
REV:	Drawing Number:
Page: 1	