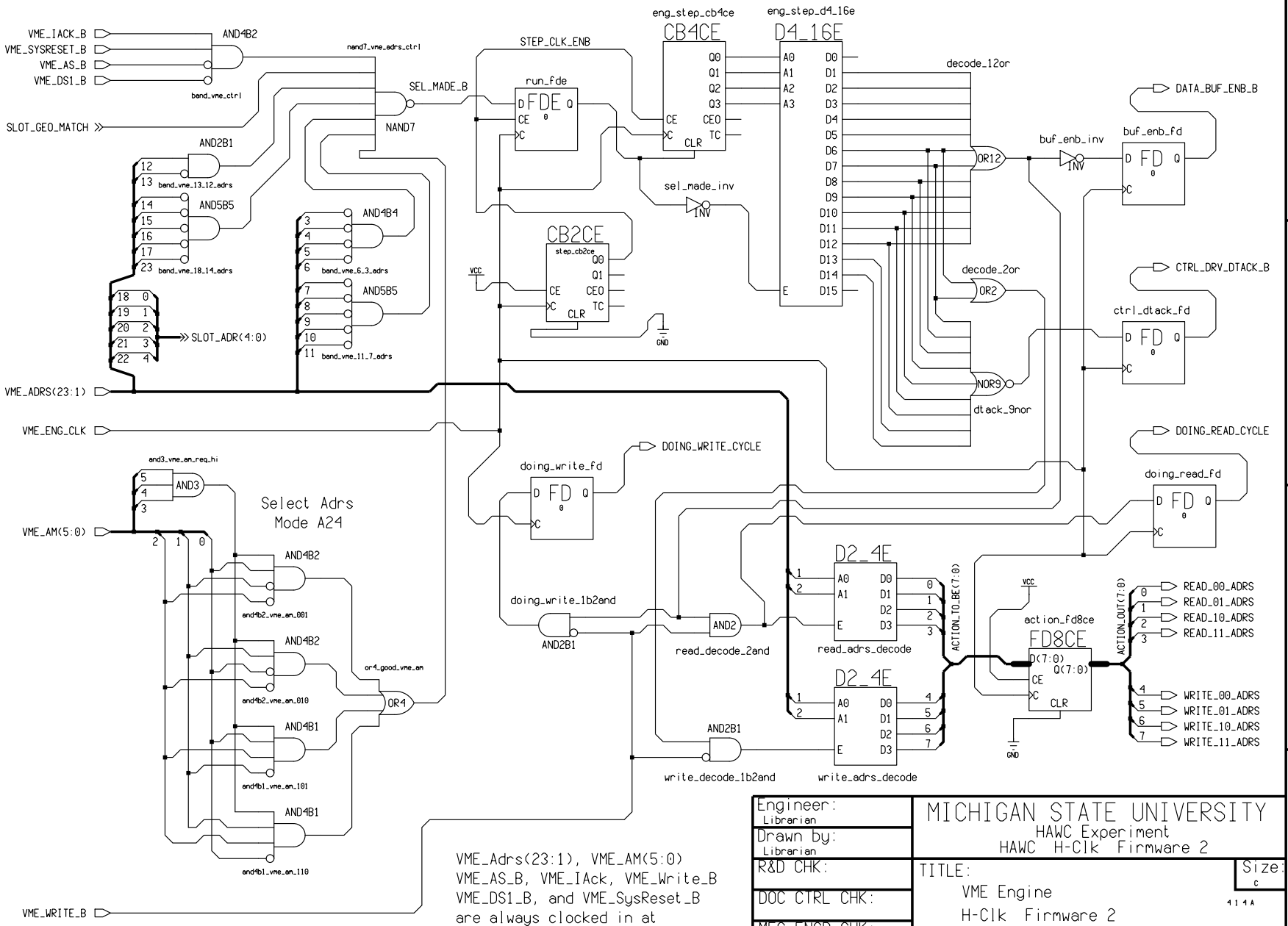
VME_IACK_B
VME_SYSRESET_B
VME_AS_B
VME_DS1_B
AND4B2
band_vme_ctrl
nand7_vme_adrs_ctrl
SLOT_GEO_MATCH
SEL_MADE_B
NAND7
STEP_CLK_ENB
run_fde
FDE
eng_step_cb4ce
CB4CE
eng_step_d4_16e
D4_16E
decode_12or
OR12
DATA_BUF_ENB_B
buf_enb_inv
INV
buf_enb_fd
FD
AND2B1
band_vme_13_12_adrs
AND5B5
band_vme_18_14_adrs
AND4B4
band_vme_6_3_adrs
AND5B5
band_vme_11_7_adrs
SLOT_ADR(4:0)
sel_made_inv
CB2CE
step_cb2ce
VCC
GND
decode_2or
OR2
CTRL_DRV_DTACK_B
ctrl_dtack_fd
NOR9
dtack_9nor
VME_ADRS(23:1)
VME_ENG_CLK
DOING_WRITE_CYCLE
doing_write_fd
DOING_READ_CYCLE
doing_read_fd
and3_vme_en_req_hi
AND3
VME_AM(5:0)
Select Adrs
Mode A24
AND4B2
and4b2_vme_am_001
AND4B2
and4b2_vme_am_010
AND4B1
and4b1_vme_am_101
AND4B1
and4b1_vme_am_110
or4_good_vme_am
OR4
doing_write_1b2and
AND2B1
AND2
read_decode_2and
D2_4E
read_adrs_decode
ACTION_TO_BE(7:0)
action_fd8ce
FD8CE
D(7:0)
Q(7:0)
CE
C
CLR
ACTION_OUT(7:0)
READ_00_ADRS
READ_01_ADRS
READ_10_ADRS
READ_11_ADRS
AND2B1
write_decode_1b2and
write_adrs_decode
WRITE_00_ADRS
WRITE_01_ADRS
WRITE_10_ADRS
WRITE_11_ADRS
VME_WRITE_B
VME_Adrs(23:1), VME_AM(5:0)
VME_AS_B, VME_IAck, VME_Write_B
VME_DS1_B, and VME_SysReset_B
are always clocked in at
the pad buffer.
Engineer:
Librarian
Drawn by:
Librarian
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:
MICHIGAN STATE UNIVERSITY
HAWC Experiment
HAWC H-Clk Firmware 2
TITLE:
VME Engine
H-Clk Firmware 2
Sheet 1 of 2
Size:
c
4144
Changed by:
Edmunds
Date Changed:
Sunday 4-Mar-2012
Time Changed:
12:00:00
QA CHK:
REV:
Drawing Number:
Page:
1 of 2