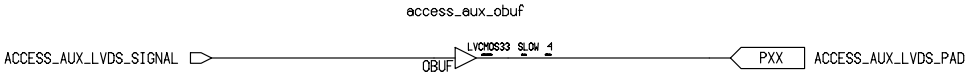
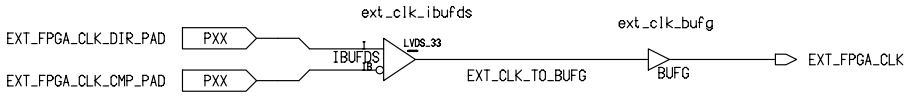


The ACCESS_AUX_LVDS signal goes to an LVDS driver. The output of this LVDS driver is the Aux LVDS signal on the Access Connector.



The Ext_FPGA_CLK signal is an LVDS signal that arrives on the Access Connector is buffered and then is received by the FPGA as LVDS.

This sheet is the FPGA's output to the Access connector's Aux LVDS signal and the FPGA's receiver for the Access connector's External Clk signal.

Changed by: Edmunds	Date Changed: Sunday 26-FEB-2012	Time Changed: 12:00:00	QA CHK:	REV:	Drawing Number:	Page: 1

Engineer: Edmunds
Drawn by: Librarian
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:

MICHIGAN STATE UNIVERSITY
HAWC Experiment
H-Clk Firmware 2

TITLE:
HAWC H-Clk Firmware 2
Aux Output and Ext Clk Input
Sheet 1 of 1

Size: C

4 1 4 A