

A Modular Readout System For A Small Liquid Argon TPC
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Abstract

A dual-FET preamplifier and a multi-channel waveform digitizer form the basis of a modular readout system for a small Liquid Argon Time Projection Chamber. Simulated signals typical of a minimum ionizing particle sampled on a 5 mm pitch can be reliably detected with a simulated detector capacitance of at least 600 pf.

Introduction

Our group is performing R&D to demonstrate the feasibility of a large multi-kiloton Liquid Argon Time Projection Chamber (LAR TPC) for neutrino oscillation, proton decay, and other experiments. The chamber will image charged particle tracks by drifting the ionization through the cryogenic liquid to a stereoscopic set of three wire planes. The track of a minimum ionizing particle in liquid Argon sampled by wires on a 5 mm pitch generates a signal corresponding $\sim 22,000$ electrons, assuming a charge collection efficiency of 90%. We wanted to show that the noise of an existing low-noise hybrid preamplifier was sufficiently low that this signal could be reliably detected under optimum conditions. To create an efficient detector, however, all external sources of noise on the signal wires, such as from HV leakage, must be held to values well below the intrinsic noise of the preamplifier studied here.

Though not optimized for this application, we used a preamplifier identical to one used by the D-Zero Tevatron Collider Run II experiment for readout of the liquid argon calorimeter. Another module used in the D0 trigger system for Run II was configured to perform a 10-bit waveform digitization and store a defined time interval of digitized data for later readout.

Under construction is a 50 liter LAR TPC that will allow observation and analysis of cosmic ray muon tracks. A sufficient number of preamplifier and waveform digitizer channels are available to readout the wire planes.

Preamplifier

The ICARUS collaboration has developed many techniques that are essential for successful operation of a LAR TPC. In their current readout electronics, signals on the wires are received by preamplifiers with an FET based front end. For the warm electronics being considered, we believe that this is still the best solution and is the one found in the low noise D-Zero dual-FET hybrid preamplifier, as pictured in Figure 1, with a circuit schematic as shown in Figure 2. Given

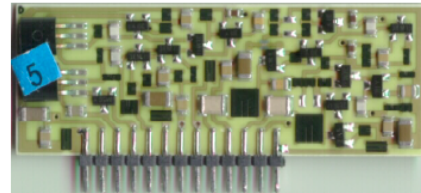


Fig. 1. LAr calorimeter preamplifier

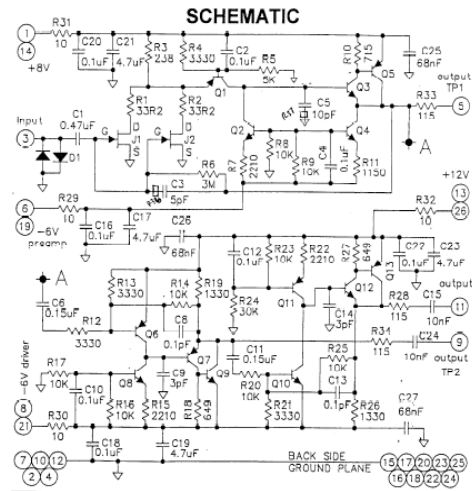


Fig. 2. Run II preamplifier circuit schematic

the similarity in the front end design, we anticipated that the performance of this preamplifier would be similar to the one used by ICARUS.

Waveform digitization

The preamplifier's output waveform is digitized by a module, the ADF-2, developed at MSU for the D0 calorimeter trigger for Run II. The ADF-2 module contains 32 channels of a modern 10-bit ADC with FPGA data control and storage. Pedestal voltage adjustment and number of other functions are performed by the module, pictured in Figure 3. A block diagram of the ADF2 digitization section is shown in Figure 4.

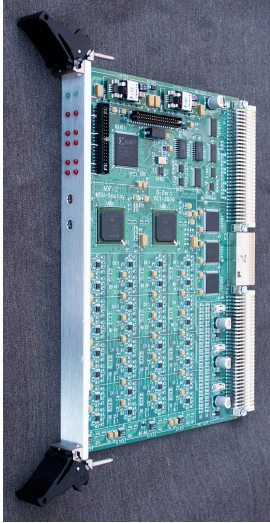


Fig. 3. ADF-2 module

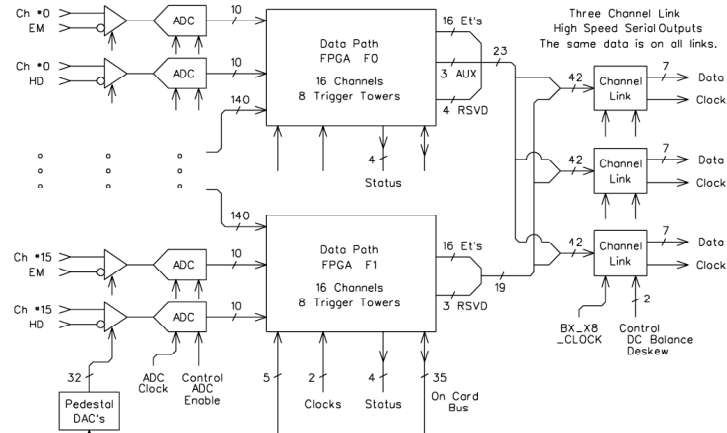


Fig. 4. ADF-2 signal processing block diagram

The module can be configured to sample a voltage at time intervals that are multiples of 33 ns (e.g., $4 \times 33 \text{ ns} = 132 \text{ ns}$) with the 10-bit digitized data stored in the available FPGA circular buffer space. With a signal rise time of about 1 μsec , we chose to sample at 197 ns intervals allowing 2048 samples to be stored in the FPGA for each channel.

Simulating the signal

Due to longitudinal diffusion a typical cluster of electrons from a minimum ionizing track arrives at the signal wires of a LArTPC with a spatial distribution having a standard deviation from near zero to $\sim 3 \text{ mm}$, and travels at a speed of $\sim 1.5 \text{ mm}/\mu\text{sec}$. Assuming a typical $\sigma = 2 \text{ mm}$, the resulting signal has the rise and fall time similar to that of a 150 KHz sine function.

The test signal used was one half cycle of a 150 KHz sine function. It represents the signal seen by a wire in the middle plane of a chamber having two induction planes and a collection plane separated by 5 mm. The first induction plane shields the signal wire from the cluster of electrons until they begin to pass through it. The peak charge seen by the amplifier occurs when the electron cluster is centered on the signal wire of the second induction plane. It will be assumed that the narrow cluster produces an induced charge equal to the 22,000 electrons of a minimum ionizing track. As the cluster

centroid approaches the collection plane, the signal drops and then disappears when the cluster of electrons is absorbed by the collection plane.

Test setup

An HP arbitrary waveform generator is used to make the half cycles of 150 KHz at the level of a couple of Volts. This signal goes through a coaxial choke as it enters a shielded preamp enclosure where it is attenuated and then goes through a set of high value resistors (to make the test signal into a current source signal) connected to the preamp input. Connected between the preamp input and ground is a silver mica capacitor to simulate the detector capacitance. Three different values of detector capacitance were used in this test: 0 pF, 330 pF, and 660 pF. Also contained in the preamp enclosure are the noise filters for the preamp power supplies and a stage of additional amplification to drive the output cable and match the input properties of the ADC.

The frequency response of the analog section is not flat at a number of points both in the preamp itself and in the amplifier between the preamp and the ADF-2 card. The high frequency and low frequency roll off in gain that were used for these tests are "reasonable" but have not been optimized. Optimizing the response of the analog section as a function of frequency requires knowing: the real signal shape, the characteristics of the noise sources, and how the signal will be analyzed in the raw ADC data. Nevertheless, the frequency spectrum of the noise seen in these tests will be presented.

The analog output signal cable from the preamp enclosure runs about 10 feet over to a VME crate that holds the ADF-2 card. The response of the ADF-2 card is basically flat across the frequencies of interest for these tests. The ADCs on the ADF-2 card are "sampling converters", i.e., when they are told to convert they sample their analog input voltage at that instant in time and then provide a digital output value that is proportional to this voltage. The VME crate is controlled by a PC through a commercial hardware interface from Bit-3. The software on the PC and the ADF-2 firmware are both derived from their corresponding elements in the D-Zero trigger control.

Test results

The waveform presented to the ADF-2 module was digitized for 400 μ sec with the time of the test pulse set at \sim 340 μ sec after the start of the digitization. Typical "traces" were recorded for each of the three test capacitances. The first 300 μ sec of each trace can be used to characterize the noise and the region around 340 μ sec to evaluate the signal plus noise. The pedestal subtracted data for four traces are overlapped and plotted as shown in Figure 5 for a 0-pf capacitance and in Figure 6 for a 600-pf simulated detector capacitance. Shown in the inset of each figure is an expanded region around the signal.

The signal to noise can be characterized by the standard deviation of the noise about zero compared to the signal amplitude. Since the noise is sensitive to the filtering that has not been optimized and other noise sources are bound to be present in a real detector we quote only approximate signal to noise ratios of \sim 20/1 for the 0-pf capacitance data and \sim 10/1 for the 600-pf simulated detector capacitance.

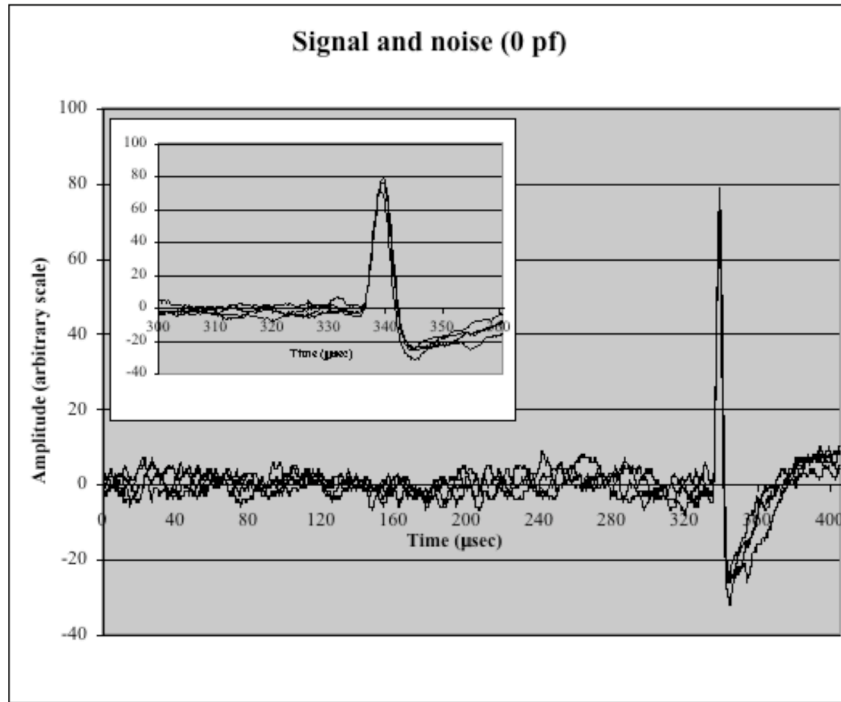


Fig. 5. Waveform for 0-pf detector capacitance

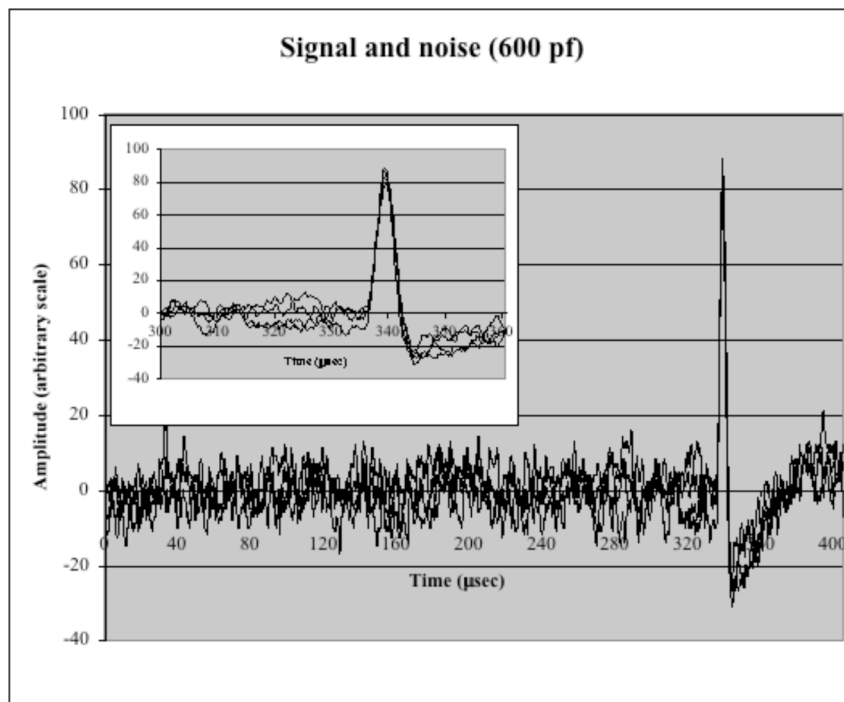


Fig. 6. Waveform for 600-pf detector capacitance

To provide more information regarding the noise we determined its power spectrum for the two detector capacitances as shown in Figure 7. A 150 kHz calibration signal with an amplitude just barely above the noise was input to the preamplifier and subtracted from the power spectra shown. It is clear from this data that the low frequency filtering could have been somewhat stronger.

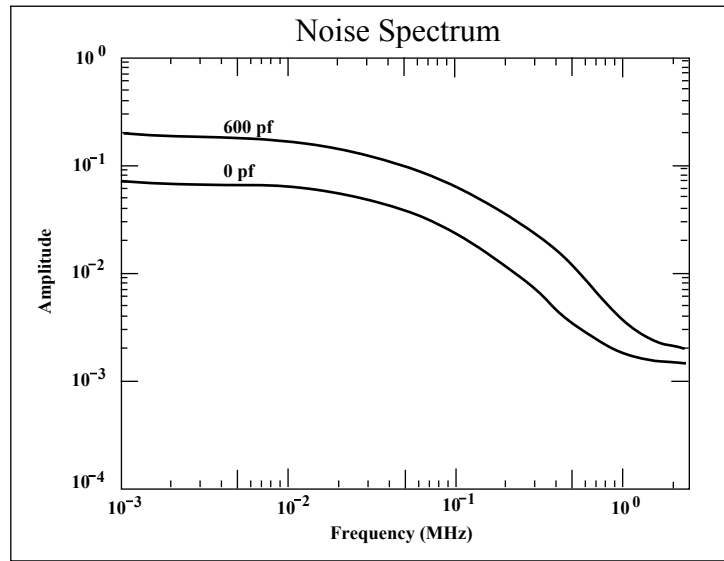


Fig. 7. Noise power for two detector capacitances.

Conclusions

It is clear that the preamplifier and ADF-2 digitizer can be used to readout the small LArTPC we are building. The 600-pf capacitance is in the range one expects for the long wires of a large detector. The data suggests that readout of a large detector will be possible utilizing techniques similar to the ones in this test. Also, it is encouraging that equipment designed for another experiment with a well established cost appears to have adequate performance for the large LArTPC detector we envision.