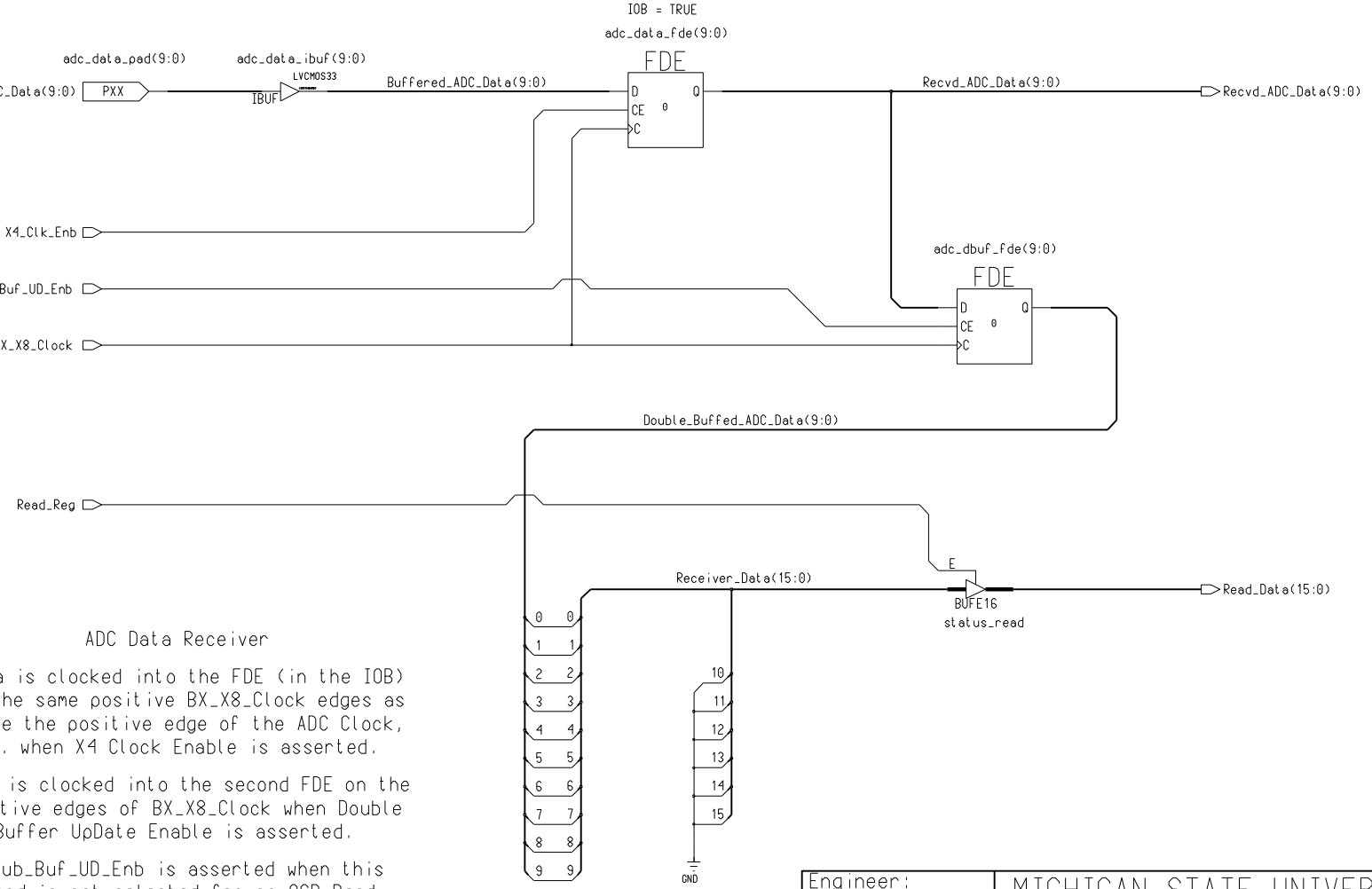

ADC Data Receiver

a is clocked into the FDE (in the IOB)
he same positive BX_X8_Clock edges as
e the positive edge of the ADC Clock,
. when X4 Clock Enable is asserted.

is clocked into the second FDE on the
tive edges of BX_X8_Clock when Double
Buffer UpDate Enable is asserted.

ub_Buf_UD_Enb is asserted when this
ard is not selected for an OCB Read
AND the X4 Clock Enable is asserted.

Read data from this register while
"Read_Reg" is asserted High.

Changed by: Edmunds	Date Changed: Wednesday 4-MAY-2005	Time Changed: 12:00:00	QA CHK:	REV:	Drawing Number:	Page: 1

Engineer: Librarian	MICHIGAN STATE UNIVERSITY D0 Run II Upgrade Run IIB L1 Calorimeter Trigger
Drawn by: Librarian	
R&D CHK:	TITLE: adc_data_receiver ADC Data Receiver for T7 Data is latched in the IO Block
DOC CTRL CHK:	Size: C
MFG ENGR CHK:	4 1 4 A