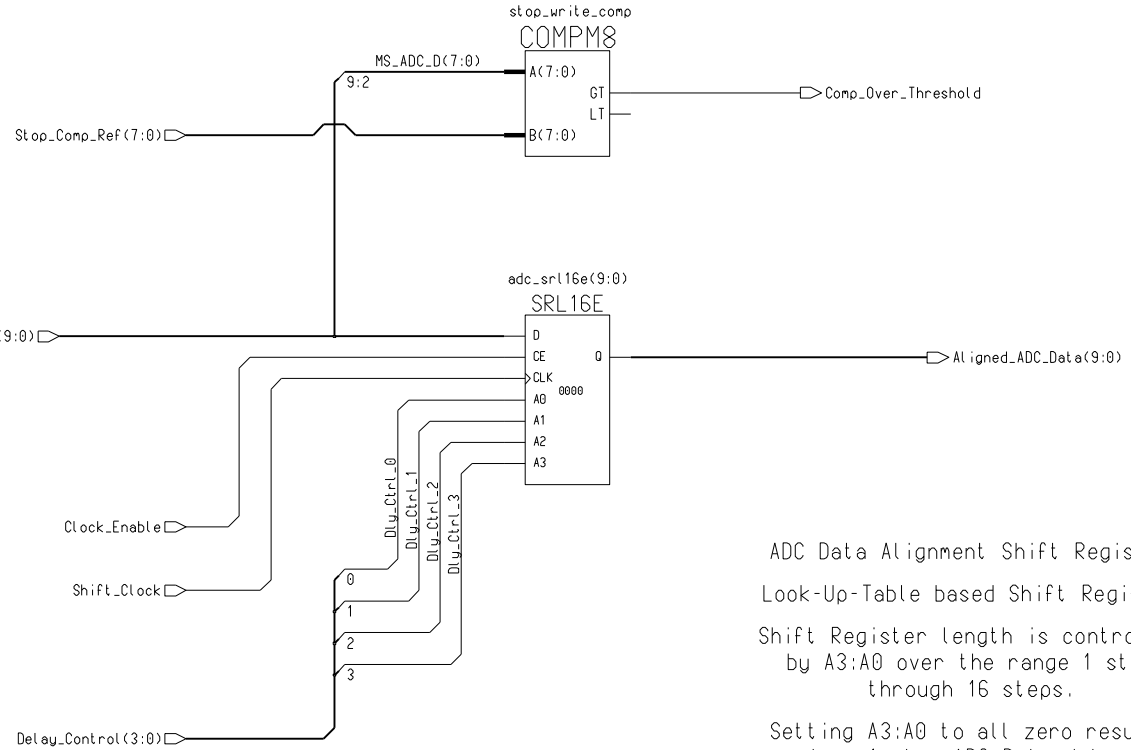
ADC Monitor Data Write Enable
Stop Comparator

BLS signal Bump has been seen.



ADC Data Alignment Shift Register

Look-Up-Table based Shift Register

Shift Register length is controlled
by A3:A0 over the range 1 step
through 16 steps.

Setting A3:A0 to all zero results
in a 1 step ADC Data delay.

The data moves on positive clock
edges only when clock enable is high.

Changed by: Edmunds	Date Changed: Tuesday 26-APR-2005	Time Changed: 12:00:00	QA CHK:	REV:	Drawing Number:	Page: 1

Engineer: Librarian	MICHIGAN STATE UNIVERSITY D0 Run II Upgrade Run IIB L1 Calorimeter Trigger
Drawn by: Librarian	
R&D CHK:	TITLE: align_adc_data Align the BLS Signal ADC Data Stop Monitor Writing Comparator
DOC CTRL CHK:	Size: C
MFG ENGR CHK:	4 1 4 A