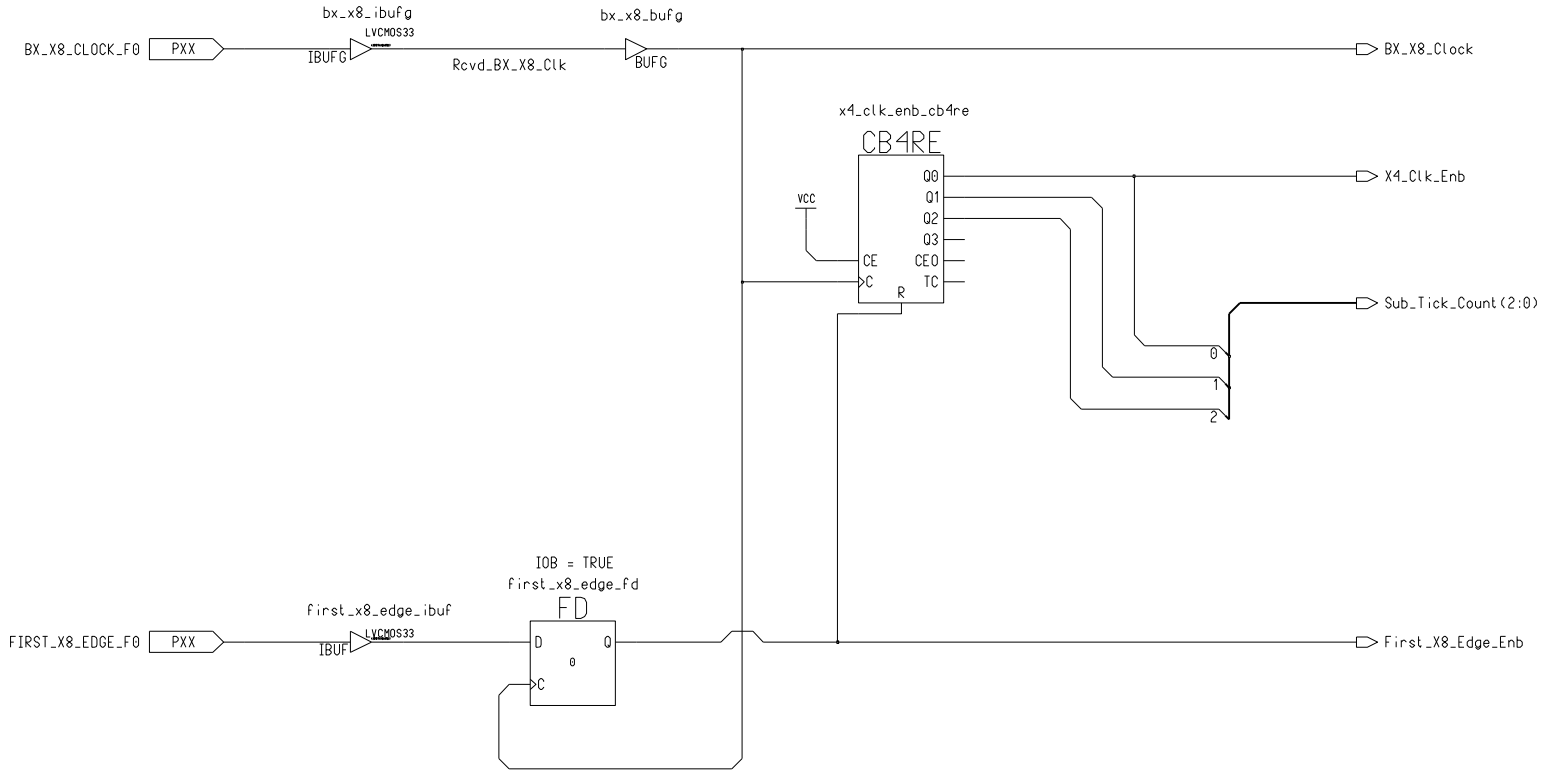

The is for the Data Path T7 design.

Clock Receiver and Distributor

The X4_Clk_Enb selects every other edge of the BX_X8_Clock. X4_Clk_Enb is a clock enable type signal.

The CB4RE has Synchronous Reset to zero.

The First_X8_Edge_Enb signal is a clock enable type signal.

Note that the positive edges of BX_X8_Clock selected by First_X8_Edge_Enb are also selected by X4_Clk_Enb.

Changed by: Edmunds	Date Changed: Thursday 28-APR-2005	Time Changed: 12:00:00	QA CHK:	REV:	Drawing Number: / Page: 1

Engineer: Librarian
Drawn by: Librarian
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:

MICHIGAN STATE UNIVERSITY
D0 Run II Upgrade
Run IIB L1 Calorimeter Trigger

TITLE:
clock_rec_dist
ADF-2 Clock Receiver
and Distributor for the T7

Size: C
4144