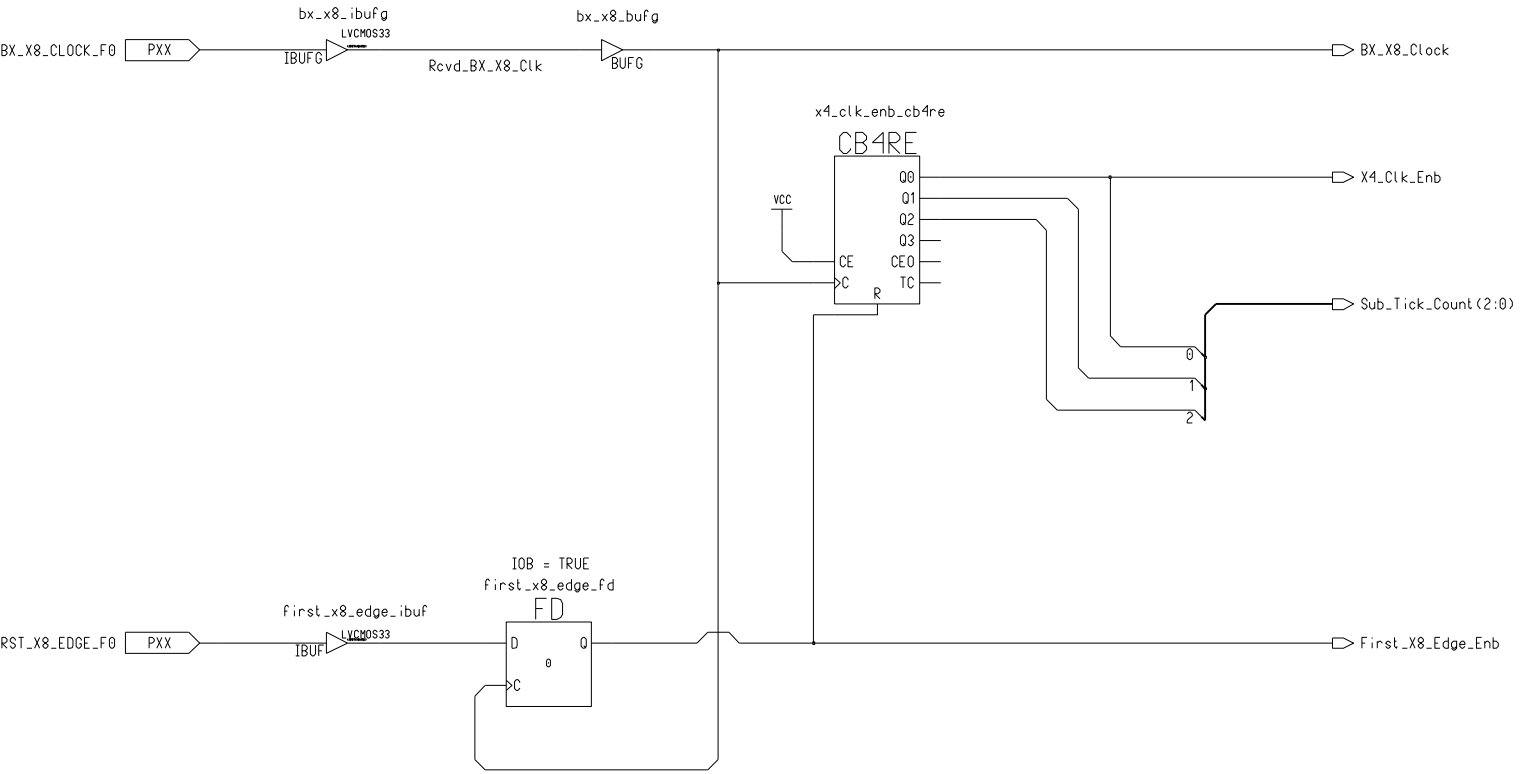


The is for the Data Path T7 design.

Clock Receiver and Distributor

The X4_Clk_Enb selects every other edge of the BX_X8_Clock. X4_Clk_Enb is a clock enable type signal.

The CB4RE has Synchronous Reset to zero.

The First_X8_Edge_Enb signal is a clock enable type signal.

Note that the positive edges of BX_X8_Clock selected by First_X8_Edge_Enb are also selected by X4_Clk_Enb.

| | | |
|---|---|---|
| Engineer: Librarian | MICHIGAN STATE UNIVERSITY<br>D0 Run II Upgrade<br>Run IIB L1 Calorimeter Trigger | |
| Drawn by: Librarian | | |
| R&D CHK: | TITLE: clock_rec_dist<br>ADF-2 Clock Receiver and Distributor for the T7 | Size: C<br>4 1 4 A |
| DOC CTRL CHK: | | |
| MFG ENGR CHK: | | |

| Changed by: | Date Changed: | Time Changed: | QA CHK: | REV: | Drawing Number: | Page: |
|---|---|---|---|---|---|---|
| Edmunds | Thursday 28-APR-2005 | 12:00:00 | | | | 1 |