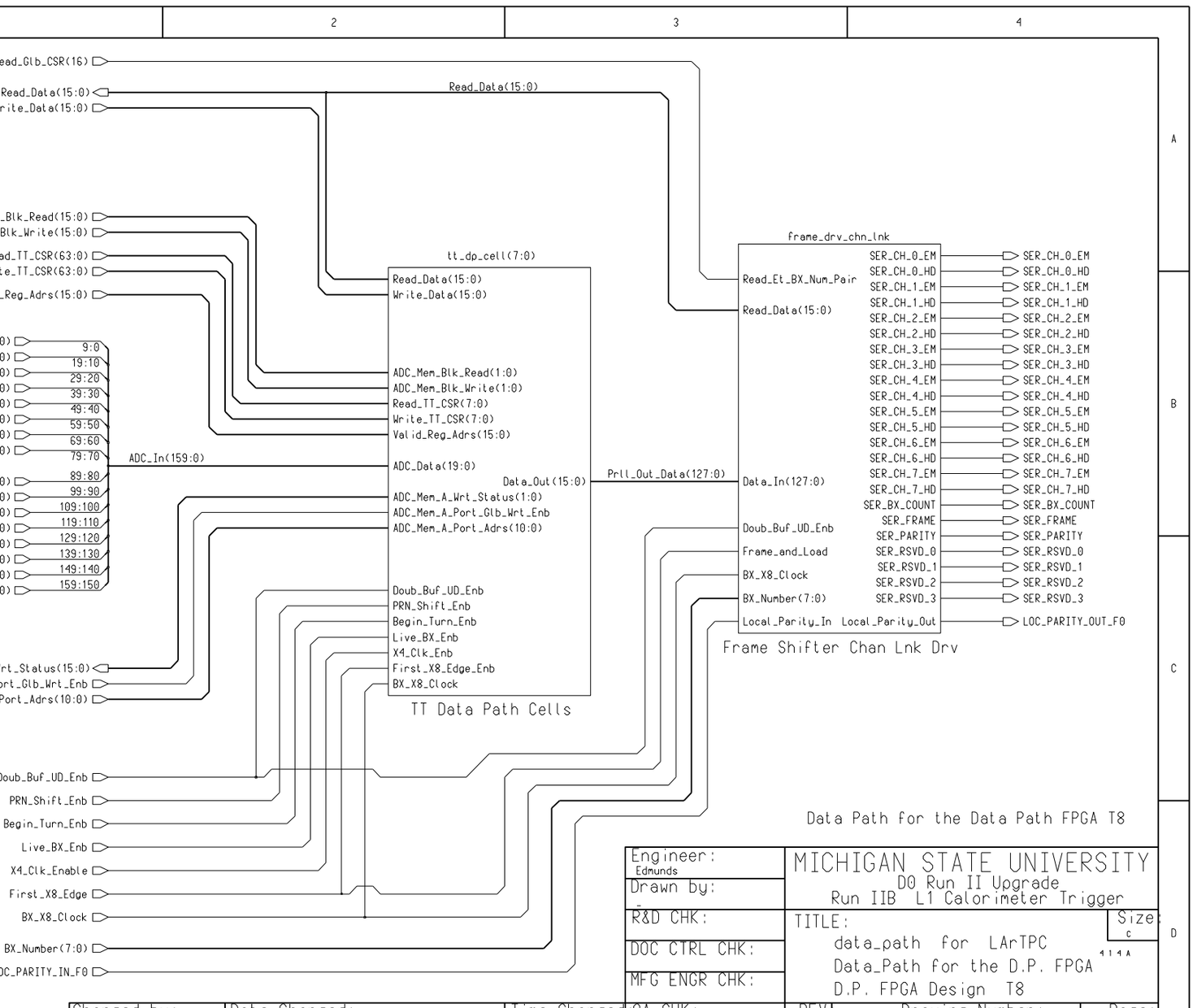
ead_Glb_CSR(16)
Read_Data(15:0)
rite_Data(15:0)
Read_Data(15:0)
_Blk_Read(15:0)
Blk_Write(15:0)
ad_TT_CSR(63:0)
te_TT_CSR(63:0)
_Reg_Adrs(15:0)
9:0
19:10
29:20
39:30
49:40
59:50
69:60
79:70
ADC_In(159:0)
89:80
99:90
109:100
119:110
129:120
139:130
149:140
159:150
rt_Status(15:0)
ort_Glb_Wrt_Enb
Port_Adrs(10:0)
Doub_Buf_UD_Enb
PRN_Shift_Enb
Begin_Turn_Enb
Live_BX_Enb
X4_Clk_Enable
First_X8_Edge
BX_X8_Clock
BX_Number(7:0)
DC_PARITY_IN_F0
tt_dp_cell(7:0)
Read_Data(15:0)
Write_Data(15:0)
ADC_Mem_Blk_Read(1:0)
ADC_Mem_Blk_Write(1:0)
Read_TT_CSR(7:0)
Write_TT_CSR(7:0)
Valid_Reg_Adrs(15:0)
ADC_Data(19:0)
Data_Out(15:0)
ADC_Mem_A_Wrt_Status(1:0)
ADC_Mem_A_Port_Glb_Wrt_Enb
ADC_Mem_A_Port_Adrs(10:0)
Doub_Buf_UD_Enb
PRN_Shift_Enb
Begin_Turn_Enb
Live_BX_Enb
X4_Clk_Enb
First_X8_Edge_Enb
BX_X8_Clock
TT Data Path Cells
Prll_Out_Data(127:0)
frame_drv_chn_lnk
Read_Et_BX_Num_Pair
Read_Data(15:0)
Data_In(127:0)
Doub_Buf_UD_Enb
Frame_and_Load
BX_X8_Clock
BX_Number(7:0)
Local_Parity_In
Local_Parity_Out
SER_CH_0_EM
SER_CH_0_HD
SER_CH_1_EM
SER_CH_1_HD
SER_CH_2_EM
SER_CH_2_HD
SER_CH_3_EM
SER_CH_3_HD
SER_CH_4_EM
SER_CH_4_HD
SER_CH_5_EM
SER_CH_5_HD
SER_CH_6_EM
SER_CH_6_HD
SER_CH_7_EM
SER_CH_7_HD
SER_BX_COUNT
SER_FRAME
SER_PARITY
SER_RSVD_0
SER_RSVD_1
SER_RSVD_2
SER_RSVD_3
LOC_PARITY_OUT_F0
Frame Shifter Chan Lnk Drv
Data Path for the Data Path FPGA T8
Engineer: Edmunds
Drawn by: -
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:
MICHIGAN STATE UNIVERSITY
D0 Run II Upgrade
Run IIB L1 Calorimeter Trigger
TITLE:
data_path for LArTPC
Data_Path for the D.P. FPGA
D.P. FPGA Design T8
Size: C
414A
Changed by: Edmunds
Date Changed: Monday 9-MAY-2005
Time Changed: 12:00:00
QA CHK:
REV:
Drawing Number:
Page: 1