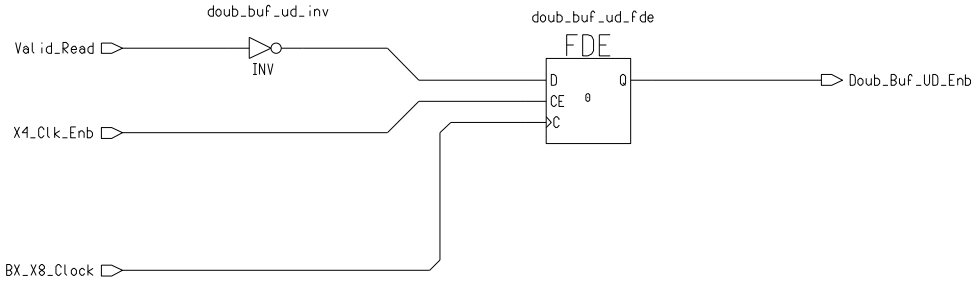

The "Double Buffer" status registers
are used to read the ADC output
values "on the fly".

Block these registers from updating
when a VME read cycle is underway.

Allow changes in the state of the
Doub_Buf_UD_Enb signal only at the
time of the update clock active edge.

I.E. all update clocks are either used
by all Double Buffer registers
or else the are completely ignored.

Engineer: Librarian	MICHIGAN STATE UNIVERSITY D0 Run II Upgrade Run IIB L1 Calorimeter Trigger
Drawn by: Librarian	
R&D CHK:	TITLE: double_buf_update_enable Double Buffer Update Enable Control used in the T7 design.
DOC CTRL CHK:	Size: C
MFG ENGR CHK:	4144A

Changed by:	Date Changed:	Time Changed:	QA CHK:	REV:	Drawing Number:	Page:
Edmunds	Friday 29-APR-2005	12:00:00				1