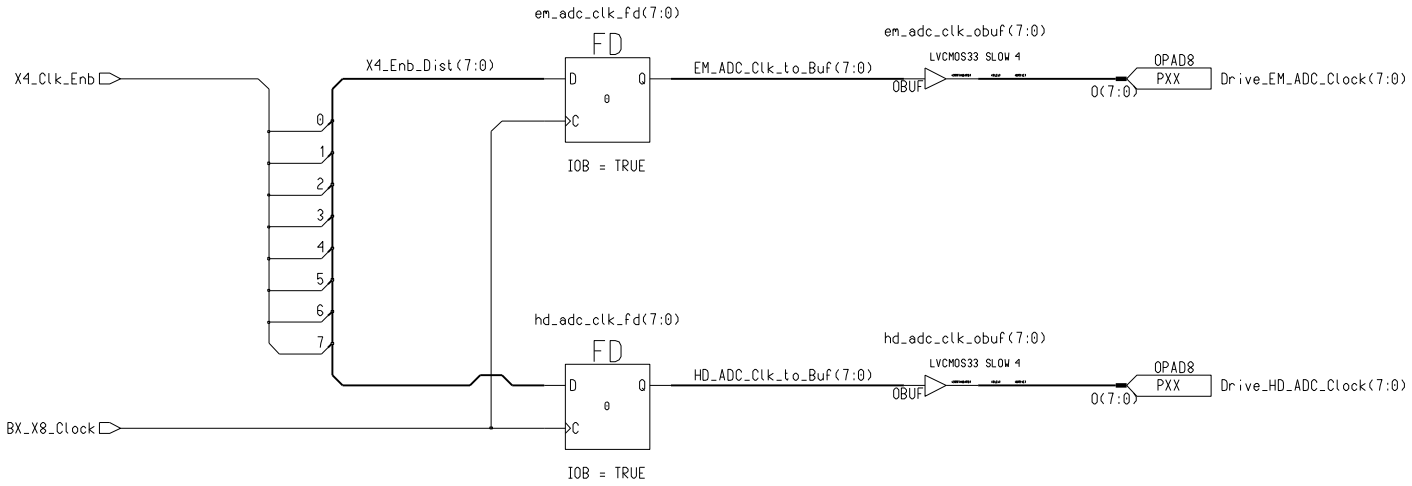

ADC Clock Generation

ADC Clock is at a 4x BX rate.

ADC Clock goes high on BX_X8 edges when X4_Clk_Enb is high.

ADC Clock Driver for T7

Changed by: Edmunds	Date Changed: Wednesday 29-DEC-2004	Time Changed: 12:00:00	QA CHK:	REV:	Drawing Number:	Page: 1

Engineer: Librarian
Drawn by: Librarian
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:

MICHIGAN STATE UNIVERSITY
D0 Run II Upgrade
Run IIB L1 Calorimeter Trigger

TITLE:
drive_adc_clock
Generate and Drive
the ADC Clock Lines

Size: C

4 1 4 A