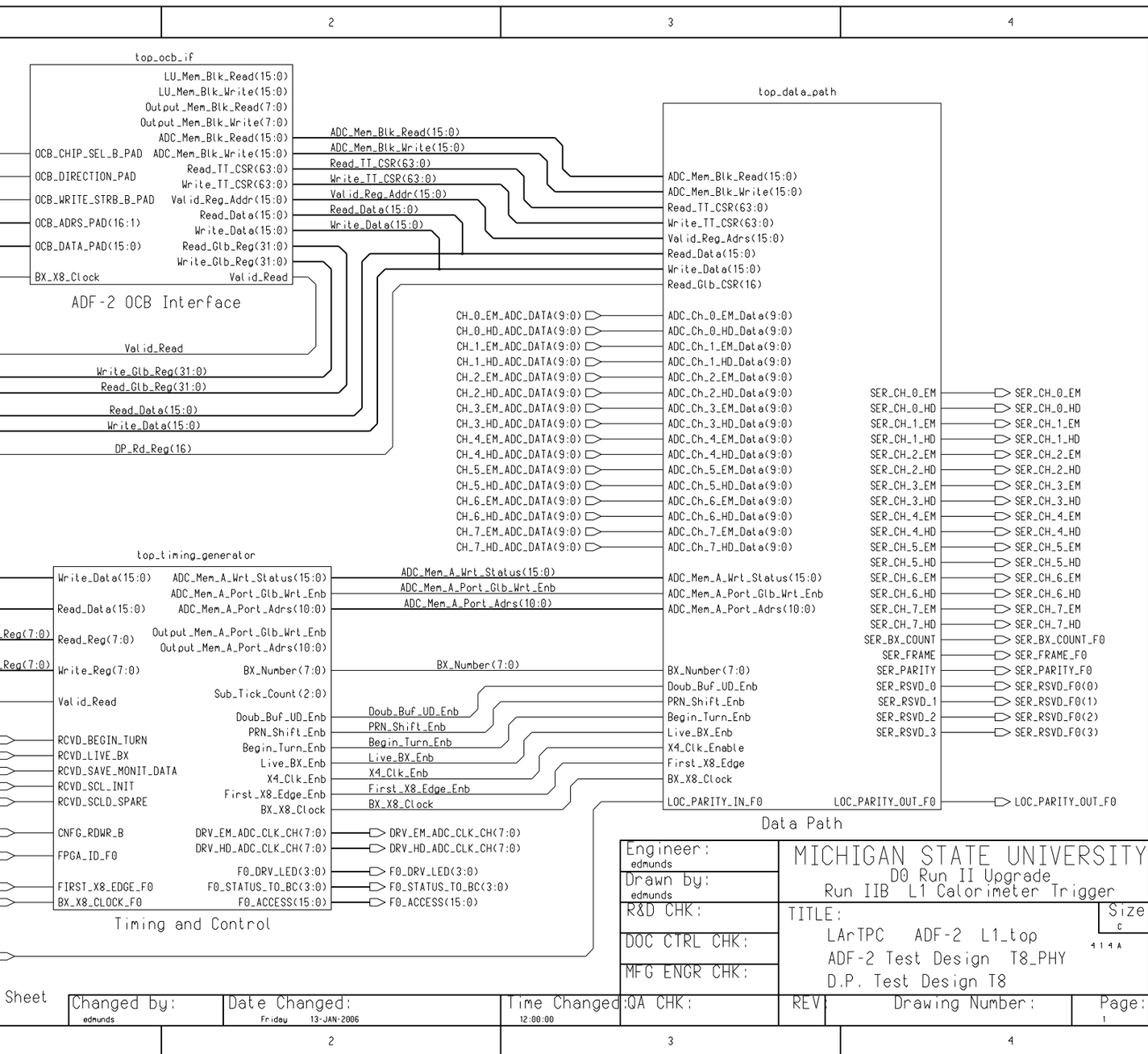
top_ocb_if
LU_Mem_Blk_Read(15:0)
LU_Mem_Blk_Write(15:0)
Output_Mem_Blk_Read(7:0)
Output_Mem_Blk_Write(7:0)
ADC_Mem_Blk_Read(15:0)
OCB_CHIP_SEL_B_PAD
ADC_Mem_Blk_Write(15:0)
Read_TT_CSR(63:0)
OCB_DIRECTION_PAD
Write_TT_CSR(63:0)
OCB_WRITE_STRB_B_PAD
Valid_Reg_Addr(15:0)
Read_Data(15:0)
OCB_ADRS_PAD(16:1)
Write_Data(15:0)
OCB_DATA_PAD(15:0)
Read_Glb_Reg(31:0)
Write_Glb_Reg(31:0)
BX_X8_Clock
Valid_Read
ADF-2 OCB Interface
ADC_Mem_Blk_Read(15:0)
ADC_Mem_Blk_Write(15:0)
Read_TT_CSR(63:0)
Write_TT_CSR(63:0)
Valid_Reg_Addr(15:0)
Read_Data(15:0)
Write_Data(15:0)
Valid_Read
Write_Glb_Reg(31:0)
Read_Glb_Reg(31:0)
Read_Data(15:0)
Write_Data(15:0)
DP_Rd_Reg(16)
top_data_path
ADC_Mem_Blk_Read(15:0)
ADC_Mem_Blk_Write(15:0)
Read_TT_CSR(63:0)
Write_TT_CSR(63:0)
Valid_Reg_Adrs(15:0)
Read_Data(15:0)
Write_Data(15:0)
Read_Glb_CSR(16)
CH_0_EM_ADC_DATA(9:0)
CH_0_HD_ADC_DATA(9:0)
CH_1_EM_ADC_DATA(9:0)
CH_1_HD_ADC_DATA(9:0)
CH_2_EM_ADC_DATA(9:0)
CH_2_HD_ADC_DATA(9:0)
CH_3_EM_ADC_DATA(9:0)
CH_3_HD_ADC_DATA(9:0)
CH_4_EM_ADC_DATA(9:0)
CH_4_HD_ADC_DATA(9:0)
CH_5_EM_ADC_DATA(9:0)
CH_5_HD_ADC_DATA(9:0)
CH_6_EM_ADC_DATA(9:0)
CH_6_HD_ADC_DATA(9:0)
CH_7_EM_ADC_DATA(9:0)
CH_7_HD_ADC_DATA(9:0)
ADC_Ch_0_EM_Data(9:0)
ADC_Ch_0_HD_Data(9:0)
ADC_Ch_1_EM_Data(9:0)
ADC_Ch_1_HD_Data(9:0)
ADC_Ch_2_EM_Data(9:0)
ADC_Ch_2_HD_Data(9:0)
ADC_Ch_3_EM_Data(9:0)
ADC_Ch_3_HD_Data(9:0)
ADC_Ch_4_EM_Data(9:0)
ADC_Ch_4_HD_Data(9:0)
ADC_Ch_5_EM_Data(9:0)
ADC_Ch_5_HD_Data(9:0)
ADC_Ch_6_EM_Data(9:0)
ADC_Ch_6_HD_Data(9:0)
ADC_Ch_7_EM_Data(9:0)
ADC_Ch_7_HD_Data(9:0)
ADC_Mem_A_Wrt_Status(15:0)
ADC_Mem_A_Port_Glb_Wrt_Enb
ADC_Mem_A_Port_Adrs(10:0)
BX_Number(7:0)
Doub_Buf_UD_Enb
PRN_Shift_Enb
Begin_Turn_Enb
Live_BX_Enb
X4_Clk_Enable
First_X8_Edge
BX_X8_Clock
LOC_PARITY_IN_F0
LOC_PARITY_OUT_F0
SER_CH_0_EM
SER_CH_0_HD
SER_CH_1_EM
SER_CH_1_HD
SER_CH_2_EM
SER_CH_2_HD
SER_CH_3_EM
SER_CH_3_HD
SER_CH_4_EM
SER_CH_4_HD
SER_CH_5_EM
SER_CH_5_HD
SER_CH_6_EM
SER_CH_6_HD
SER_CH_7_EM
SER_CH_7_HD
SER_BX_COUNT
SER_FRAME
SER_PARITY
SER_RSVD_0
SER_RSVD_1
SER_RSVD_2
SER_RSVD_3
SER_CH_0_EM_F0
SER_CH_0_HD_F0
SER_CH_1_EM_F0
SER_CH_1_HD_F0
SER_CH_2_EM_F0
SER_CH_2_HD_F0
SER_CH_3_EM_F0
SER_CH_3_HD_F0
SER_CH_4_EM_F0
SER_CH_4_HD_F0
SER_CH_5_EM_F0
SER_CH_5_HD_F0
SER_CH_6_EM_F0
SER_CH_6_HD_F0
SER_CH_7_EM_F0
SER_CH_7_HD_F0
SER_BX_COUNT_F0
SER_FRAME_F0
SER_PARITY_F0
SER_RSVD_F0(0)
SER_RSVD_F0(1)
SER_RSVD_F0(2)
SER_RSVD_F0(3)
LOC_PARITY_OUT_F0
Data Path
top_timing_generator
Write_Data(15:0)
ADC_Mem_A_Wrt_Status(15:0)
ADC_Mem_A_Port_Glb_Wrt_Enb
Read_Data(15:0)
ADC_Mem_A_Port_Adrs(10:0)
Read_Reg(7:0)
Output_Mem_A_Port_Glb_Wrt_Enb
Output_Mem_A_Port_Adrs(10:0)
Write_Reg(7:0)
BX_Number(7:0)
Sub_Tick_Count(2:0)
Valid_Read
Doub_Buf_UD_Enb
PRN_Shift_Enb
RCVD_BEGIN_TURN
Begin_Turn_Enb
RCVD_LIVE_BX
Live_BX_Enb
RCVD_SAVE_MONIT_DATA
X4_Clk_Enb
RCVD_SCL_INIT
First_X8_Edge_Enb
RCVD_SCLD_SPARE
BX_X8_Clock
CNFG_RDWR_B
DRV_EM_ADC_CLK_CH(7:0)
FPGA_ID_F0
DRV_HD_ADC_CLK_CH(7:0)
F0_DRV_LED(3:0)
FIRST_X8_EDGE_F0
F0_STATUS_TO_BC(3:0)
BX_X8_CLOCK_F0
F0_ACCESS(15:0)
Timing and Control
ADC_Mem_A_Wrt_Status(15:0)
ADC_Mem_A_Port_Glb_Wrt_Enb
ADC_Mem_A_Port_Adrs(10:0)
BX_Number(7:0)
Doub_Buf_UD_Enb
PRN_Shift_Enb
Begin_Turn_Enb
Live_BX_Enb
X4_Clk_Enb
First_X8_Edge_Enb
BX_X8_Clock
DRV_EM_ADC_CLK_CH(7:0)
DRV_HD_ADC_CLK_CH(7:0)
F0_DRV_LED(3:0)
F0_STATUS_TO_BC(3:0)
F0_ACCESS(15:0)
Engineer: edmunds
Drawn by: edmunds
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:
MICHIGAN STATE UNIVERSITY
D0 Run II Upgrade
Run IIB L1 Calorimeter Trigger
TITLE:
LArTPC ADF-2 L1_top
ADF-2 Test Design T8_PHY
D.P. Test Design T8
Size: C
4144
Sheet
Changed by: edmunds
Date Changed: Friday 13-JAN-2006
Time Changed: 12:00:00
QA CHK:
REV:
Drawing Number:
Page: 1