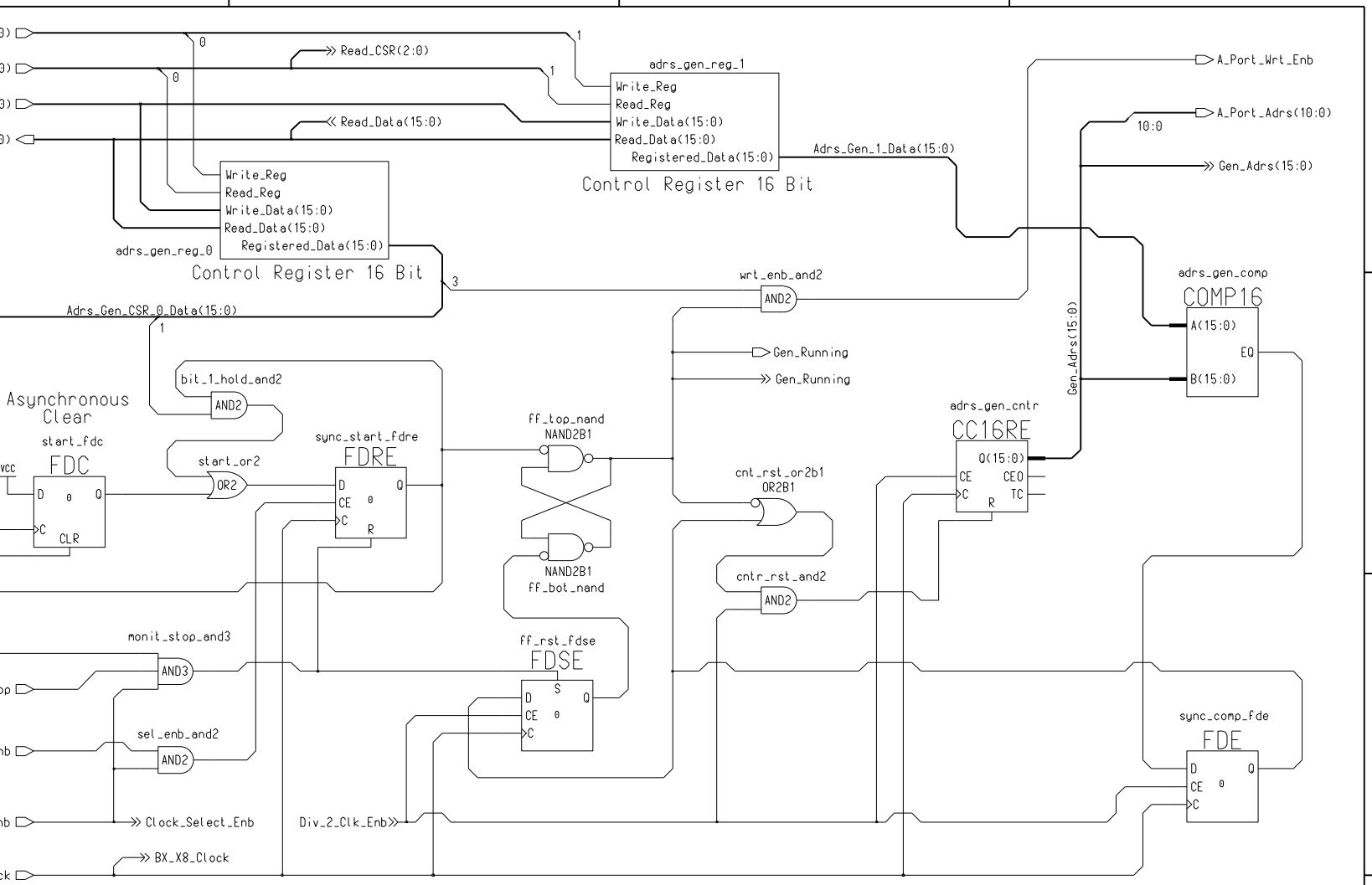

for LArTPC Page #1 of 2

r the async Start signal from TCC.
ync up with the Begin_of_Turn.
sert the "A" Port Write Enable.
he Write Adrs from 0 through COMP value.
drs Gen only at end of count sequence.
nit_Stop causes an immediate stop.

Set and Reset of FDSE and FDRE do not require an asserted CE. All operations are synchronous.

CC16RE all synchronous. Reset overides increment. Reset does not require CE.

Changed by: Edmunds	Date Changed: Monday 16-JAN-2006	Time Changed: 12:00:00	QA CHK:	REV:	Drawing Number:	Page: 1

Engineer: Librarian
Drawn by: Librarian
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:

MICHIGAN STATE UNIVERSITY
D0 Run II Upgrade
Run IIB L1 Calorimeter Trigger

TITLE:
mem_a_port_adrs_ctrl
Memory "A" Port Write Address and Global Control for T7

Size: c
4 1 4 A