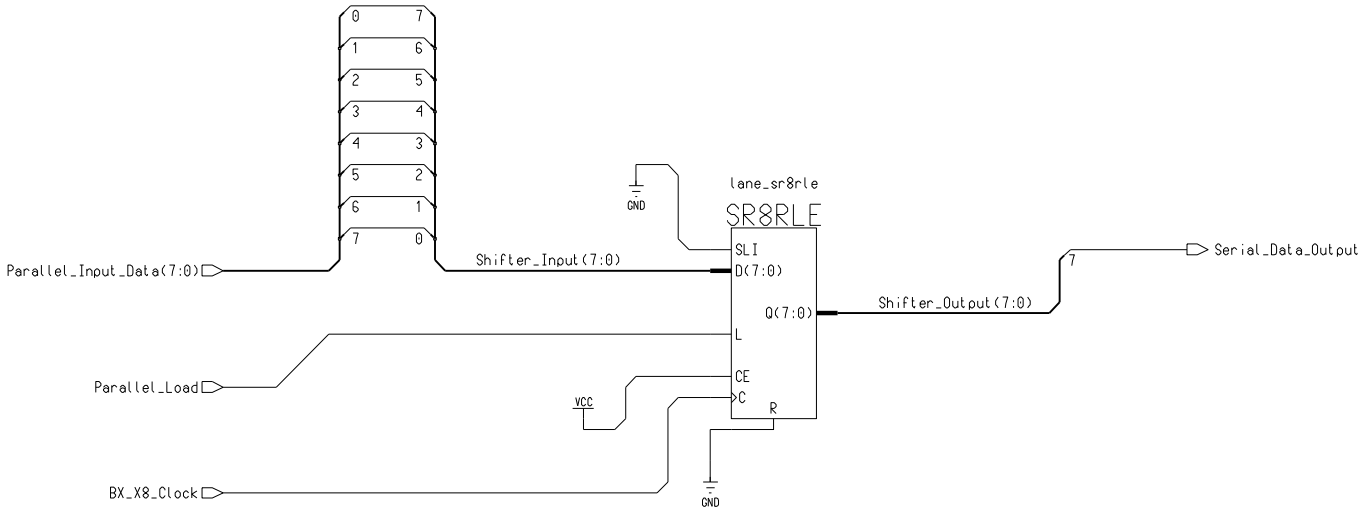
Reverse the order of the Loaded data
so that the LSB comes out first.



Shifter for one lane of Channel Link output

The SR8RLE is a Left Shift component,
i.e. Q7 shfts out first and then Q6, Q5, ...

For ADF to TAB we need the LSB to shift out first.
This is accomplished by loading the parallel data
into the SR8RLE in backwards order.

In the SR8RLE the LOAD operation overrides the SHIFT operation.
Clock Enable is not required for the LOAD operation.

All operations are synchronous and there is an operation
on every cycle of the BX_X8_Clock.

T6 Shifter for One Lane

Engineer: Librarian	MICHIGAN STATE UNIVERSITY D0 Run II Upgrade Run IIB L1 Calorimeter Trigger	
Drawn by: Librarian		
R&D CHK:	TITLE: shifter for one lane One Lane of Channel Link Output D.P. FPGA Design T6	Size: C 414A
DOC CTRL CHK:		
MFG ENGR CHK:		

Changed by:	Date Changed:	Time Changed:	QA CHK:	REV:	Drawing Number:	Page:
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