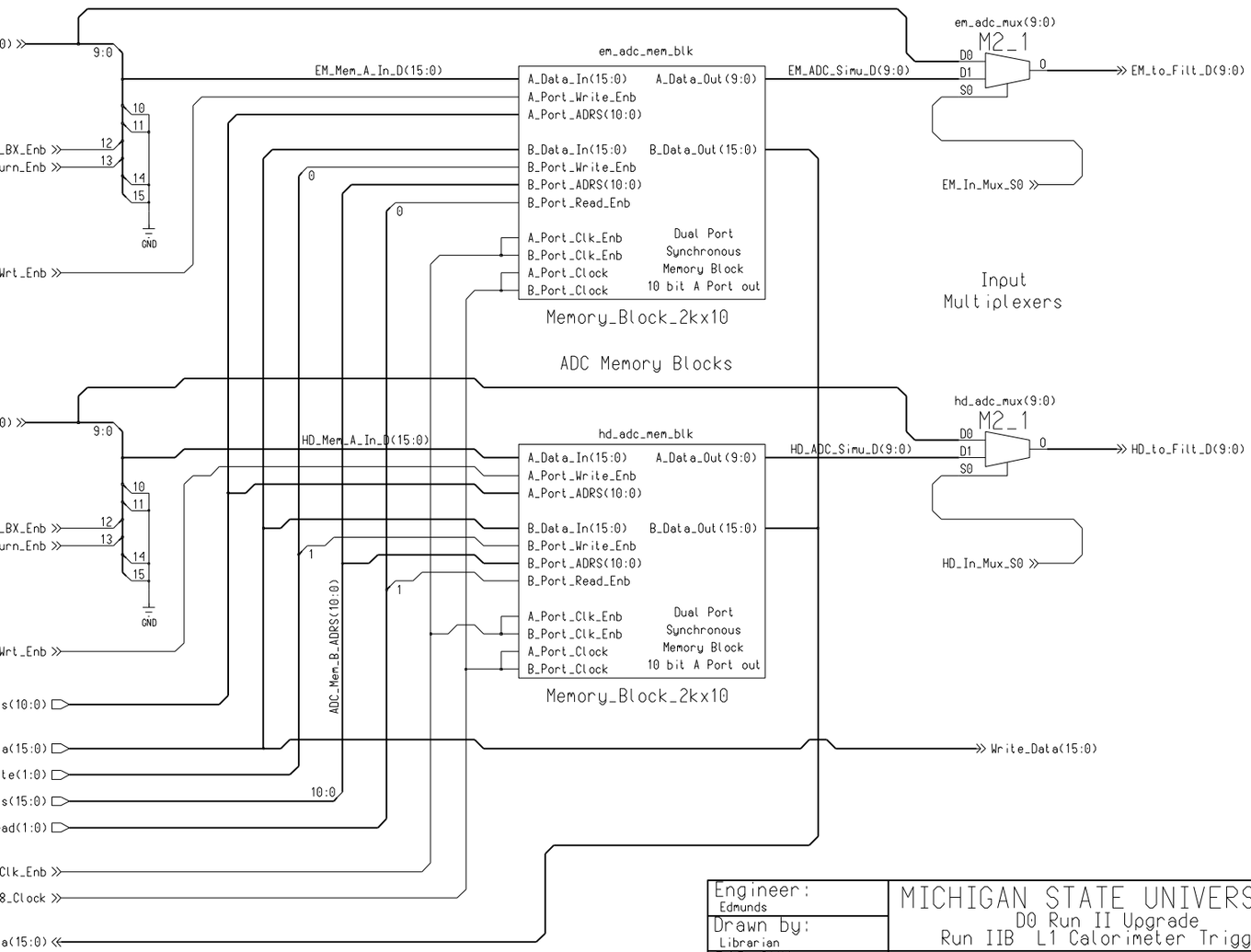

Trigger Tower Cell of Data Path Page 2 of 9
ADC Block Memory - Monitor and Simulation Data
Input Multiplexer

Engineer: Edmunds	MICHIGAN STATE UNIVERSITY D0 Run II Upgrade Run IIB L1 Calorimeter Trigger
Drawn by: Librarian	
R&D CHK:	TITLE: tt_cell for LArTPC Trigger Tower Cell of Data Path D.P. FPGA Design T7
DOC CTRL CHK:	Size: C
MFG ENGR CHK:	4144

Changed by:	Date Changed:	Time Changed:	QA CHK:	REV:	Drawing Number:	Page:
Edmunds	Friday 29-APR-2005	12:00:00				2