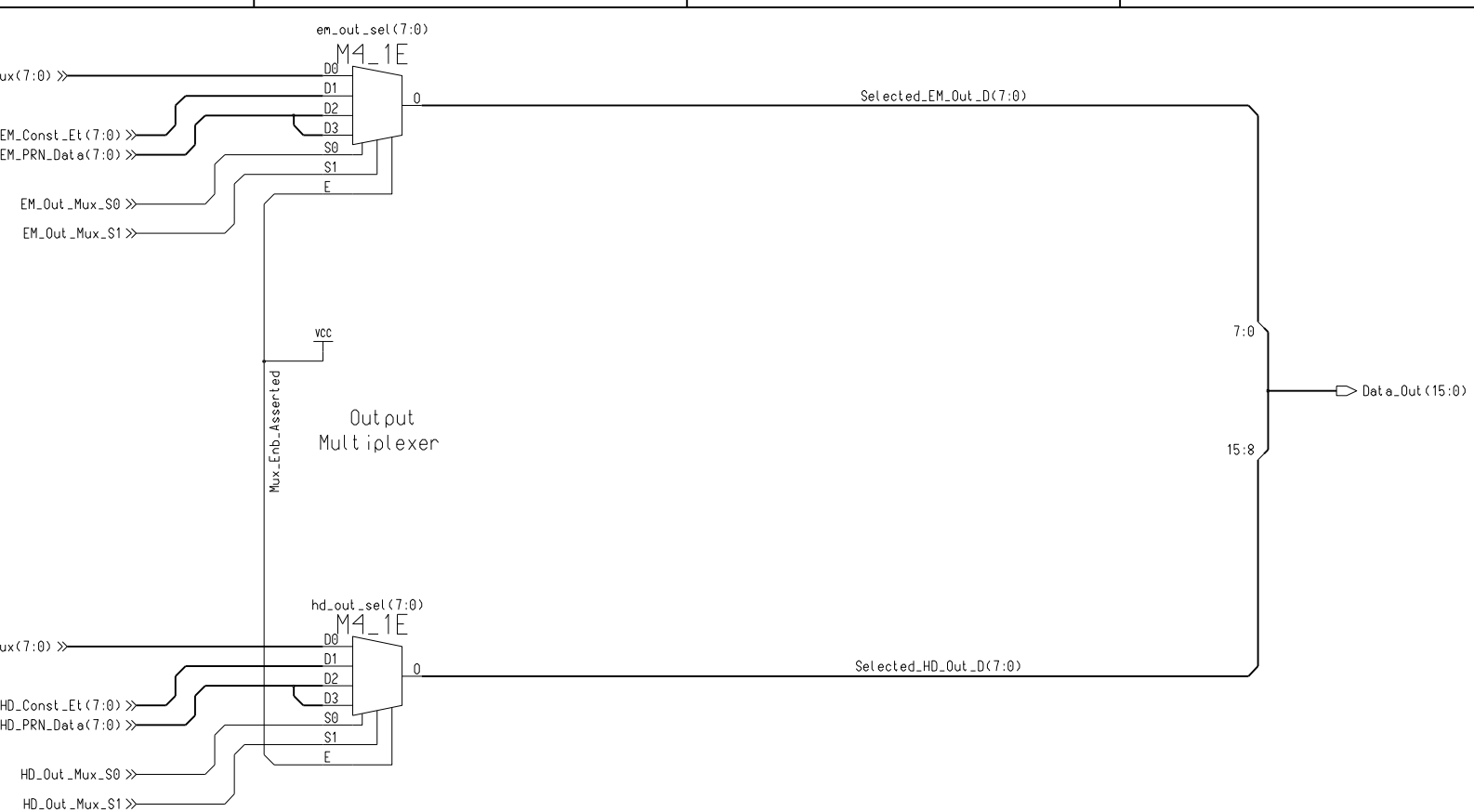

Trigger Tower Cell of Data Path Page 3 of 9

Output Multiplexer

This sheet had the Final Output Memory Block

Final Output Memory Block is not used in L1 for LArTPC

irst_X8_Edge_Enb → First_X8_Edge_Enb

Engineer: Edmunds	MICHIGAN STATE UNIVERSITY D0 Run II Upgrade Run IIB L1 Calorimeter Trigger		
Drawn by: Librarian			
R&D CHK:	TITLE: tt_cell for LArTPC Trigger Tower Cell of Data Path D.P. FPGA Design T7	Size: C	
DOC CTRL CHK:			
MFG ENGR CHK:			
Changed by: Edmunds	Date Changed: Friday 13-JAN-2006	Time Changed: 12:00:00	QA CHK:
REV:	Drawing Number: 4141A	Page: 3	