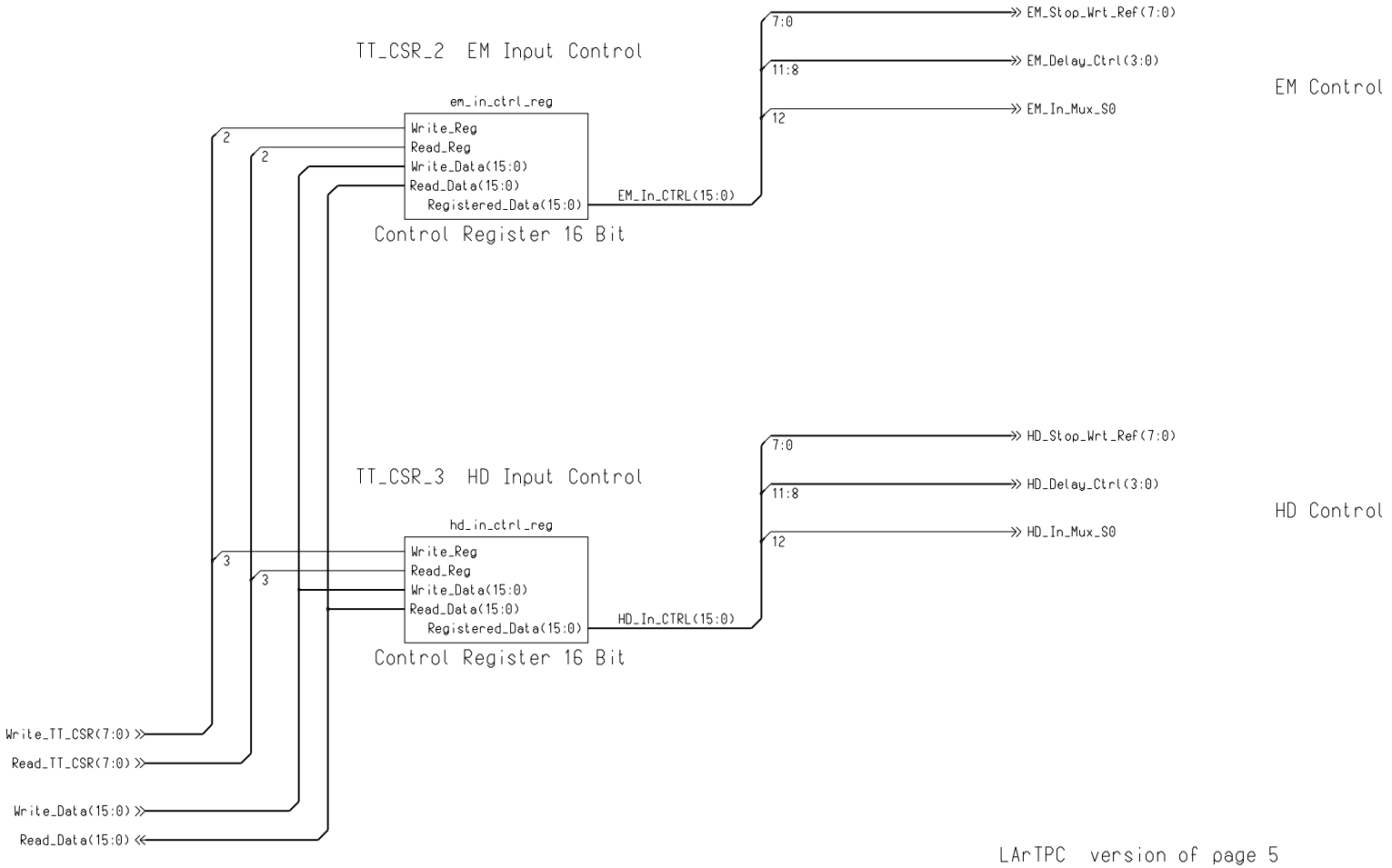

LArTPC version of page 5

Trigger Tower Cell of Data Path Page 5 of 9

TT Input Section Control

Control of the ADC Data Delay, Comparator Threshold for Stopping ADC Monitor Data Writes, the Input Multiplexer, and of the Mode of Stopping ADC Monitor Data Writing.

Engineer: Edmunds	MICHIGAN STATE UNIVERSITY D0 Run II Upgrade Run IIB L1 Calorimeter Trigger
Drawn by: Librarian	
R&D CHK:	TITLE: tt_cell for LArTPC Trigger Tower Cell of Data Path D.P. FPGA Design T7
DOC CTRL CHK:	Size: C
MFG ENGR CHK:	4141A

Changed by:	Date Changed:	Time Changed:	QA CHK:	REV:	Drawing Number:	Page:
Edmunds	Tuesday 17-JAN-2006	12:00:00				5