LArTPC DAQ Tests Using Existing D-Zero Electronics

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The purpose of this presentation is to describe some of the LArTPC DAQ test that we have done using existing D-Zero electronics components. The goal is to verify that these components could be used as the DAQ system for a small test LArTPC system at Fermilab. Short descriptions of these tests are provided in the following paragraphs.

- Basic Noise Level Tests

  The dual FET Run II D-Zero Preamp was used in the input stage of our test system. Mounted on the same circuit board with this preamp is a post amplifier and filter. This filter provides band pass filtering of approximately the correct frequency range for signals from an LArTPC detector with 5mm grid spacing.

  From the output of the post amplifier filter the analog signal travels through several meters of differential cable to the input of the D-Zero ADF-2 card. The ADF-2 card receives the differential analog signal and digitizes it with a 10 bit ADC that was typically setup to provide one sample every 200 nsec. Within FPGAs on the ADF-2 card these digital samples are recorded in a circular buffer with 2048 storage locations. When triggered, the writing of data into this circular buffer is stopped and the recorded data can be readout over the VME Bus connection with the ADF-2 card. The ADF-2 card provides 32 channels of this functionality.

  The data from the ADF-2 card is readout into a computer which can provide such functions as plotting it, or Fourier transforming the 2048 sample records to frequency space, or calculating the RMS of the sample record for noise measurement.

- Standard Test Signal

  To get an idea of how well the system described above would work with LArTPC level signals we determined a "standard" test signal to use with this equipment to simulate the wire signal from the LArTPC detector. The intent was to simulate a middle induction plane wire signal where charge would first flow into the preamplifier and then flow back out of it. The test signal that we settled on is a single cycle of 150 kHz sin wave. This signal is scaled so that over 3.33 usec approximately 22,000 electrons flow into the preamplifier and then over the next 3.33 usec they flow back out.

  We recorded many examples of this test signal using different value mica capacitors shunting the preamplifier input to ground. The intent was to make a semi quantitative measurement of the signal to noise ratio that the D-Zero dual FET preamplifier would provide with a LArTPC level input signal at various values of detector capacitance. The filtering provided by the post amplifier filter was not optimized but rather just provided approximate the correct band pass range.

- Effect of Detector Wire Resistance

  Because of the high resistance of the small diameter SS wire typically used in LArTPC detectors (approximately 90 Ohms/meter for 4mil 304V SS wire) we were concerned about the noise that very long wires might cause in the system. In order to study the effect of the long wire resistance in a compact laboratory setup we have modeled the distributed wire resistance and shunt capacitance with lumped values. Our test setup typically uses 15 resistors and capacitors in the model of the detector wire. This detector wire model is connected to the input of the preamplifier and readout electronics that was described above.

  We can see the Johnson noise from the wire resistance. As expected, because this is a distributed resistance and shunt capacitance, the level of this noise is less than that seen when all of the capacitance is located at the far end of the resistive wire. We have not yet studied the effect of multiple wires with coupling between them.

  We will also study the change in signal shape depending upon whether the test signal is injected close to the preamplifier or near the far end of the wire. In either case the preamplifier will collect all of the charge but we expect to see slower signals when the test signal is injected near the far end of the wire.

- Preamplifier Mother Board

  Because the noise level seen in the tests described above appear to be low enough to see real LArTPC signals with the D-Zero dual FET preamplifier we are now designing a small circuit board to hold 16 channels of preamplifier and post amplifier filter. This card also holds the passive components for Bias Voltage and test signal distribution. This preamplifier mother board is designed so that its analog output signals will plug directly into the ADF-2 card. Output connectors are provided so that we may either use all 32 channels on the ADF-2 card, and thus have 2048 circular buffer storage locations per channel, or use only every other channel on the ADF-2 card, and thus have 4096 storage locations per channel. We plan on assembling enough of these preamplifier mother boards to provide a few hundred channels of test system DAQ.