ARIANNA: the Icarus experiment readout module

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Abstract

Icarus detector is a liquid Argon Time Projection Chamber that requires continuous signal recording for each channel to provide three dimensional images of any ionizing event. A complete drift volume imaging of the next 600 ton module will result in 1.15 Gbit, with a data rate of 1.15 Tbit/s. The collected data can be highly reduced by recognizing Regions Of Interest (ROI) of the signal by means of a custom hit finding unit (DAEDALUS) working pipelined in the data acquisition path. DAEDALUS is an ASIC that implements an algorithm developed for hit detection and proven to be very efficient both on real and on simulated data.

Since only ROI's are saved in memory and contiguous regions can be correlated to enhance detector self triggering capability, a high efficiency zero skipping is obtained in real time.

A VME board hosting 16 Icarus digital channels has been designed and built as a demonstrator for functionality and performance test.

The board, named ARIANNA, and DAEDALUS chip are here presented in detail.

I. Introduction

The Icarus project aims to build a multi-kiloton liquid Argon Time Projection Chamber (TPC) to be operated in the Gran Sasso Laboratory (Italy) to search for rare underground phenomena such as proton decay and neutrino oscillations [1, 2, 3].

The detector is essentially a large cryogenic pool equipped with an electronic readout system. Ionizing events taking place in the volume, where a uniform electric field is applied, will produce free electrons that will drift parallel to the field inducing a current on the electrodes. The readout is performed with a chamber consisting of a number of parallel wire planes located at the end of the drift volume. This experimental technique offers a "bubble-chamber" quality of events but the detector is continuously sensitive and self-triggerable and sufficiently safe to be located underground [4].

As a part of R&D programme small volume detectors have been extensively studied and a medium scale prototype with a mass of 3 ton has been built at CERN [5]. The detector has collected data from June 1991 to October 1995 and the parameters that determine the behaviour of the detector have been measured [6].

The Icarus collaboration is now going to build a first 600 ton detector module with a volume of approximately 7.2x3.9x19.9 m^3 [7]. The cryostat has four readout chambers with a maximum drift length of 1.5 m and a maximum electrons collection time of the order of 1 ms. Each readout plane has three readout coordinates at 60^o from each other and a readout wire pitch of 3 mm that leads to a total amount of about 46000 wires.

The front-end electronics lies outside the dewar and consists of a custom low noise amplifier followed by a 16 input analog multiplexer that works up to 40 MHz with 10 bit accuracy. The multiplexer drastically reduces to about 2875 the number of channels needed to transfer data to the control room, where the digital readout system is located. Both the amplifier and the multiplexer are custom ASIC designed in 0.8 μm BiCMOS technology [8].

The readout system is structured as a multichannel waveform recorder that stores the charge information collected by each sense wire during the drift of the electrons. Since the detector is continuously sensitive, given the resolution both in space and time, a complete drift volume image results in 1.15 Gbit, at a drift speed of 1.5 mm/μs, giving a data rate of 1.15 Tbit/s. In order to optimize the memory usage a signal feature extractor unit (DAEDALUS) has been designed and introduced in the DAQ path [9]. The unit is able to command memory writing through the recognition of Regions Of Interest (ROI) of the signal directly while digitizing data. A ROI has been defined as a time window around a signal rising edge (hit). Only data around the detected peaks is then stored for a later offline analysis.

ARIANNA is a 16 channel readout module prototype designed and built in VME standard as a demonstrator for functionality and performance test. Since DAEDALUS chip processes in parallel 4 adjacent channel signals, four chips serve the set of 16 channels on the board. In the following a description of ARIANNA and DAEDALUS functionality is reported.

II. ARIANNA Module

The signals from a set of 16 channels are converted by a single ADC after passing the 16 to 1 analog multiplexer, as indicated in figure 1. Both the multiplexer and the ADC work at 40 MHz, so the ADC converts every 25 ns a single channel signal among the 16 adjacent multiplexed, giving a 400 ns sampling time on each channel.

Digitized data is input into the Dual Port RAM, organized in circular buffers, and into the DAEDALUS chips where it is analysed. The CKSYNC signal is used to keep synchronization between the analog multiplexing and the digital demultiplexing realized inside the chips.

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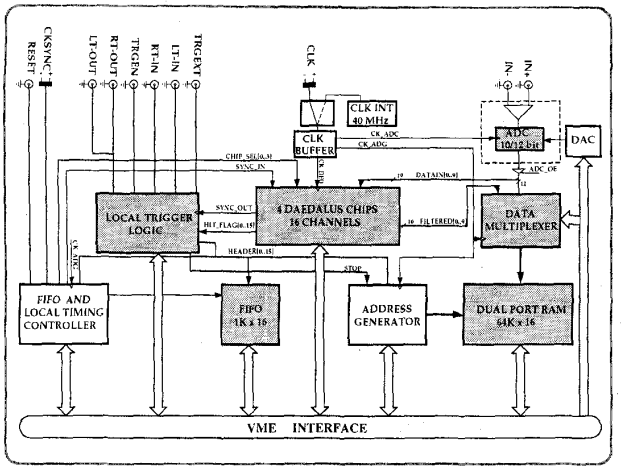

Figure 2 : ARIANNA block diagram.

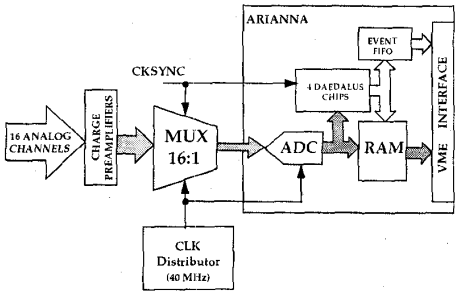

Figure 1 : ARIANNA functional description.

The presence of a hit on a channel induces a buffer saving and the memorization on the FIFO of some information useful for event reconstruction. The Dual Port RAM and the FIFO are accessible through VME [10].

In figure 2 the module block diagram is given. Functional blocks have been highlighted and are here described.

A. The A/D section

The A/D section has been placed on a small piggy back board in order to test several solutions, such as different ADC performances and 10/12 bit resolution. Burr Brown and Analog Devices ADC have been tested and performances are comparable. However at the moment Burr Brown 10/12 bit devices seem to be more suitable because of their pin to pin compatibility. In fact it could be necessary to increase the A/D range to avoid signals pile up.

The ADC input is differential, with a full scale input range of 1 V. The signal offset is adjustable through a 12 bit DAC that allows the regulation over the whole range of the analog signal.

B. The DAEDALUS chip

DAEDALUS chip implements an algorithm developed for hit detection [11]. Typical Icarus signals are voltage steps rising in a few microseconds and with a much slower decay; feature extraction is based on the recognition of the rising edge. A time-sliding window strategy has been adopted. Inside a time window of programmable fixed size a positive slope is searched for computing the differences between every two consecutive signal samples: positive values are accumulated while negative and zero values are separately counted [12].

During this search another time window, variable in size, mirrors the first one keeping memory of the same sum values.

When the fixed size window overlaps a rising edge the positive sum increases its value while the negative and zero values keep low. The slope is recognized looking at threshold conditions on both sum value and negative and zero counts. Once the hit has been recognized, the second window fixes its lower bound and continues to accumulate the positive differences, stretching its size step by step, until it covers the whole rising edge. The accumulated differences inside the stretched window mirror the signal rising edge.

A nonrecursive median filter with programmable order (up to 15 samples) is first applied to the signal to reduce high frequency noise while preserving sharp edges. In figure 3 an Icarus collection signal, the median filter result and the sum of the differences accumulated inside the stretched window (called filtered output) are shown.

The chip has been realized in 0.7 μm CMOS technology on a 4.4x4.4 mm^2 silicon area and it works up to 50 MHz [13]. The complete block diagram is given in figure 4.

It operates in parallel on four adjacent channel signals, so 4 chips serve the set of 16 channels on the board. Its architecture is pipelined at 1/16 of the external clock frequency. Data (10 bit) is input and output at the clock frequency into the same channel; latency depends on the median filter order and on the

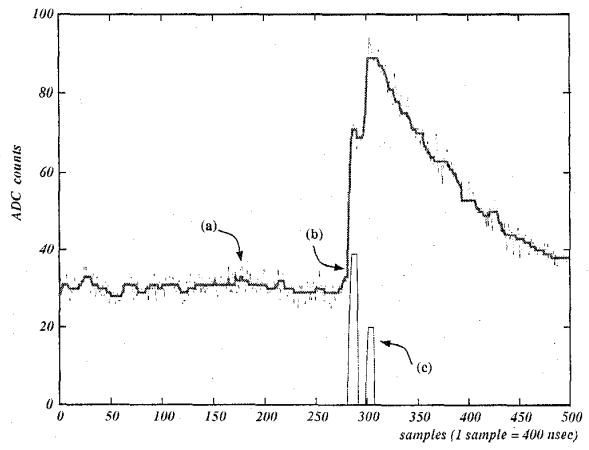

Figure 3 : Icarus collection signal (a) before and (b) after the median filter; (c) DAEDALUS filtered output.

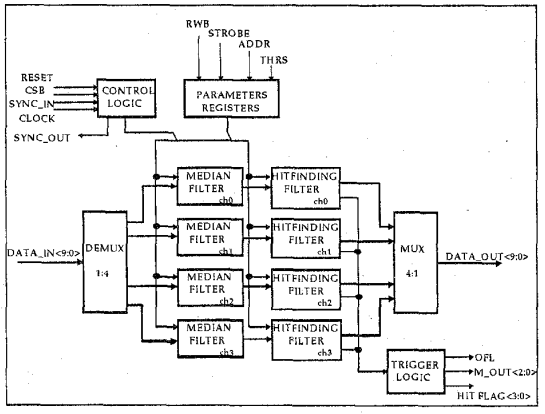

Figure 4 : DAEDALUS block diagram.

time window size chosen for feature extraction. All mentioned thresholds correspond to programmable parameters. Edge detection is stated for every channel through a "HIT FLAG" signal.

DAEDALUS chip is fully testable since it has been designed following the design rules for testability with the stuck-at-faults model and it has a fault coverage around 100%.

On the readout board the four chips share the ADC output bus (as indicated in figure 5) and the input and output data rate matches with the A/D conversion rate of 40 MHz.

Data is input into the chip enabled by the ChipSel signal while filtered data is collected from the same chip (see timing in figure 6). HIT FLAG signals are input at 2.5 MHz into the Local Trigger Logic giving single channel peaks information in order to generate the trigger signal. The DAEDALUS SYNC_OUT signal going low flags when a group of 16 channel filtered data is ready. It is input as clock into the Local Trigger Logic and the first active signal is generated after a latency time from the first valid CKSYNC signal. At the 40 MHz working frequency, latency ranges from 2.8 μs to 14 μs.

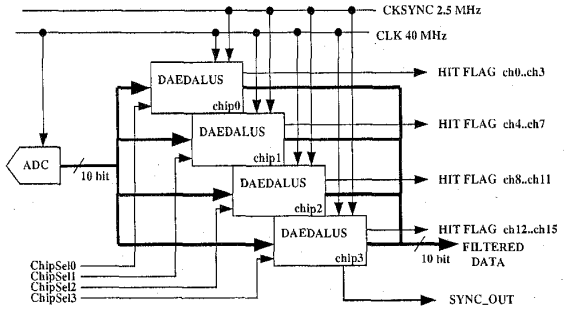

Figure 5 : DAEDALUS chips connection.

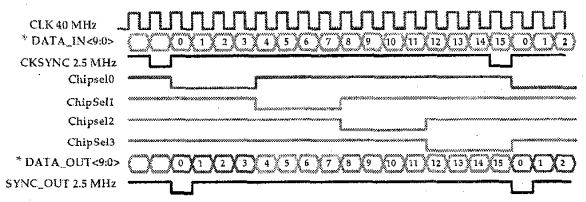

Figure 6 : DAEDALUS input/output data timing.

C. *The data multiplexer*

Digitized data passes through a multiplexer before entering the RAM that is organized in buffers of 16 bit words. It is possible to choose the data format into the RAM simply setting through VME two control bits. Allowable configurations are:

- 10 bit ADC data + 6 bit of DAEDALUS filtered output (5 MSB and the OR of the last 5 as LSB);
- 12 bit ADC data + 4 bit of DAEDALUS filtered output (3 MSB and the OR of the last 7 as LSB);
- 10 bit DAEDALUS filtered output.

The last configuration is used only to test the chips functionality.

The multiplexer has been implemented with an Altera programmable device, so a pattern generator has been also provided inside for DAEDALUS test.

D. *The Dual Port RAM*

The Dual Port RAM is organized in programmable length circular buffers. For each channel a minimum size of 128 bytes and a maximum size of 8 Kbytes have been provided. The maximum size has been dimensioned to collect a maximum drift length inside the detector.

The converted data is recorded in the active write buffer and the write pointer is automatically incremented; the read pointer is controlled through VME, allowing recover of an event while the acquisition is in progress.

A trigger signal, generated by the Local Trigger Logic, commands memory writing of a number of samples around the HIT position (ROI). A few samples around the hit are in fact necessary to extract offline the relevant parameters from the digitized data: peak time, that gives the track position inside

the volume; pulse height, which is proportional to the track ionization; rise time, that depends both on track angle and on the distribution of the electron cloud.

In figure 7 the structure of a buffer is shown. *Nbuf* is the number of samples inside the buffer while *Npre* samples before the trigger signal and *Npost* samples between the end of the trigger and the end of the buffer are the minimum values required for the analysis. *Nbuf*, *Npre* and *Npost* are parameters programmable through VME.

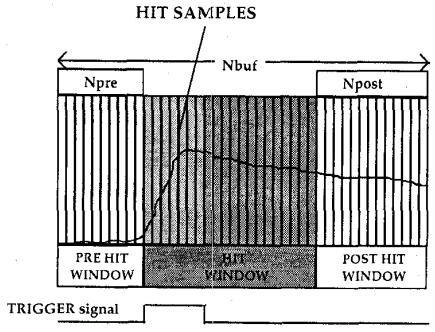

Figure 7 : Structure of a buffer into the RAM.

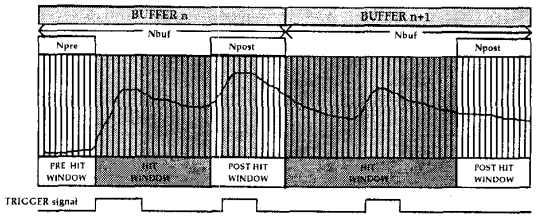

Figure 8 : Example of two buffers saved in attachment.

If the trigger signal exceeds in length the *HIT WINDOW* or a new trigger is generated inside the *POST HIT WINDOW*, another buffer is saved in attachment to the first one (figure 8). This avoids overlapping buffers and assures continuous trigger sensibility. Referring to the example of figure 8, the peak detected in the *POST HIT WINDOW* of the first buffer is completely saved inside the buffer but the *Npost* samples requirement is not respected. Another buffer is then immediately saved attached to the first one. The second buffer saved contains also all the information needed to analyse the peak detected inside its *HIT WINDOW*, so this trigger signal will be ignored.

E. The Local Trigger logic

The block is implemented with a Xilinx FPGA and it generates the trigger signal that commands memory writing combining the foreseen trigger sources in order to achieve different auto-trigger configurations (figure 9). Possible trigger sources are an external trigger (TRGEXT), the 16 HIT FLAG signals from DAEDALUS chips and the two adjacent boards local triggers (RT_IN and LT_IN). The external trigger is prevalent and is always active while an enable signal (TRGEN) has been provided for all the other sources. DAEDALUS HIT FLAG signals originate two different triggers: the logical OR of all the flags and the MAJORITY trigger (n/16 flags set at the same time, with the threshold n programmable). RT_IN and LT_IN board input should be connected to the LT_OUT and RT_OUT output of the adjacent boards, in order to propagate to the nearest groups a trigger found by DAEDALUS chips on a group of 16 channels.

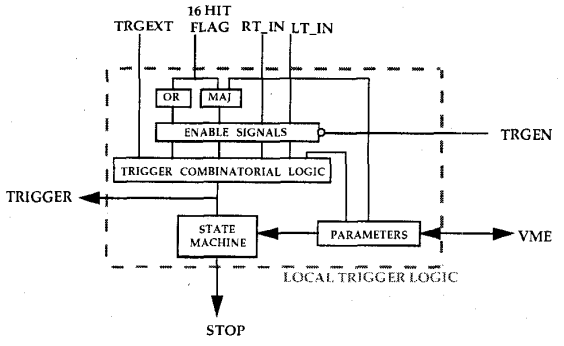

Figure 9 : Local Trigger logic block diagram.

In the same block a specialized state machine has been inserted to check for the presence of triggers and to generate the *STOP* signal, that is the timing correct *"change buffer"* signal. It is necessary in fact to take into account the buffer size chosen, the number of samples needed around the peak and the current DAEDALUS chips latency in order to save into the buffers the exact number of samples after the beginning of the trigger. Otherwise, being the buffer circular, some samples might be overwritten and information lost. All the parameters are input through VME. The machine also keeps memory of triggers arrived during a buffer saving and generates additional *STOP* signals when needed.

F. The FIFO

For each buffer saved in memory, five 16 bit words are written on the FIFO:

- the absolute time value correspondent to the last sample saved in memory;
- the write memory stop pointer address;
- the buffer dimension;
- the trigger source;
- the 16 HIT FLAG signals.

Time reference is necessary to correlate different buffers relative to the same event. The stop pointer address allows the correct reconstruction of the circular buffer, since the first data in the buffer is not always the first saved in time. An information is also saved on the source that originates the trigger as it could be a combination of many. The HIT FLAG signals give an "image" of the channel status inside the buffer.

III. EVENT EXAMPLES

In the following two Icarus events are presented. They have been collected at the smallest prototype built (50 litres) during

the 1997 test at the CERN neutrino beam.

The images represent a set of 128 collection (below, light grey) and 128 induction (above, dark grey) signals. On the left of the images the complete event is shown in the analog form (more dark grey corresponds to higher signals). This would be stored in memory if the hit finding procedure is not applied on the signals but all the data from the detector is saved. On the right the reduced event is shown. Only a suitable number of samples around the hit position found by DAEDALUS are saved into memory.

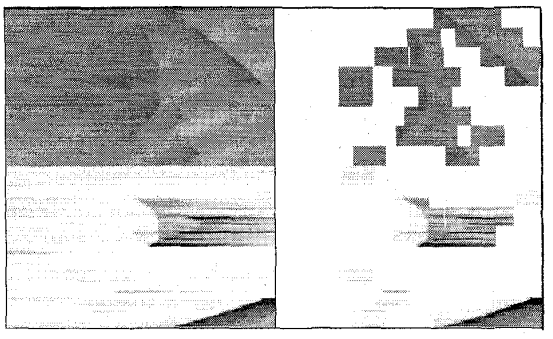

Figure 10 : Collection and induction image of an event (left) before and (right) after DAEDALUS filtering. Horizontal coordinate is drift time.

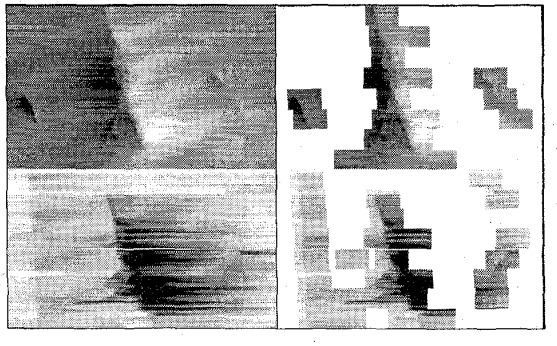

Figure 11 : Collection and induction image of an e.m. shower (left) before and (right) after DAEDALUS filtering. On the left of the image a cosmic ray track is also clearly visible. Horizontal coordinate is drift time.

A complete event takes 256 Kbytes of memory. The reduced event in figure 10 only 77.8 Kbytes (30% of the complete size) and the one in figure 11 only 98.3 Kbytes (the 38% of the complete size). The fully reconstructed events after offline analysis are shown in figure 12.

IV. Conclusions

Few prototypes of the module described have been produced and extensively tested since June 1997.

DAEDALUS chips perform according to the specifications.

The final version of the module ARIANNA is now in development; it will be a 9U VME board and it will deal with larger number of input channels (up to 96).

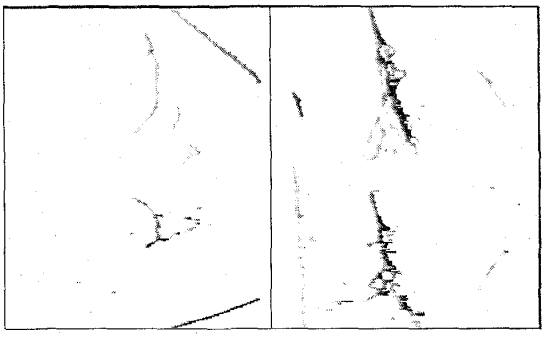

Figure 12 : Events reconstructed after offline analysis: on the left the event of figure 10, on the right the event of figure 11.

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