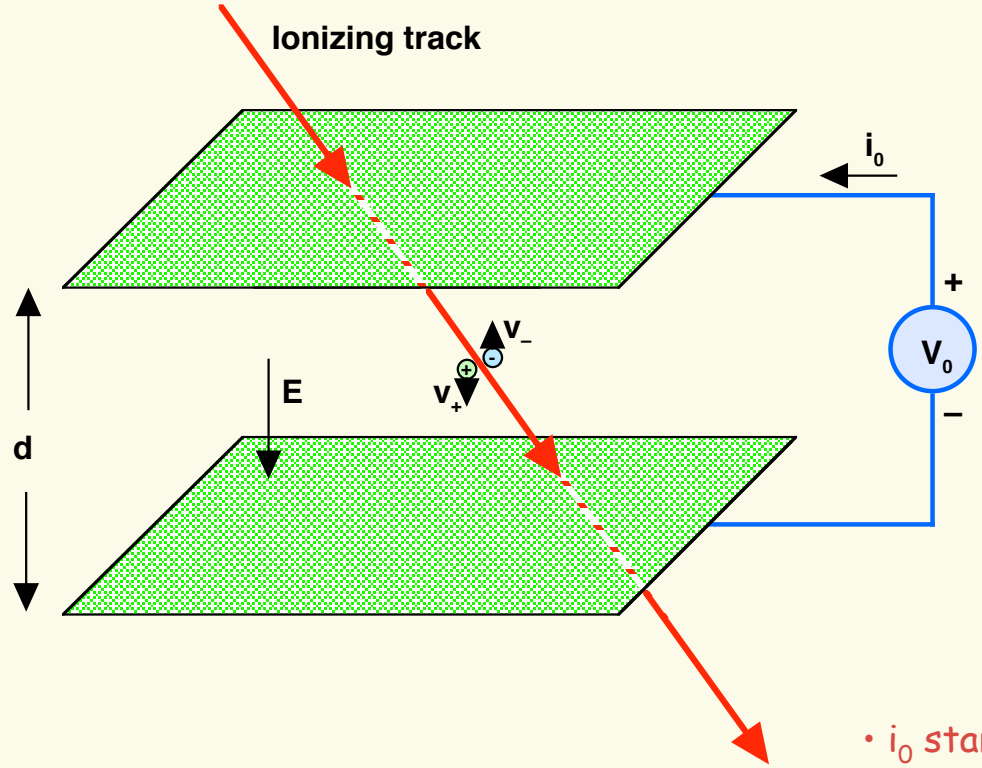
The ICARUS read-out system

- ✓ 3D Imaging in the ICARUS LAr-TPC
- ✓ Layout, optimization and performance of front-end electronics (analogue + digital)
- ✓ Self-triggering and zero-suppression
- ✓ DAQ software, on-line display and monitoring

The ionization chamber (LAr)



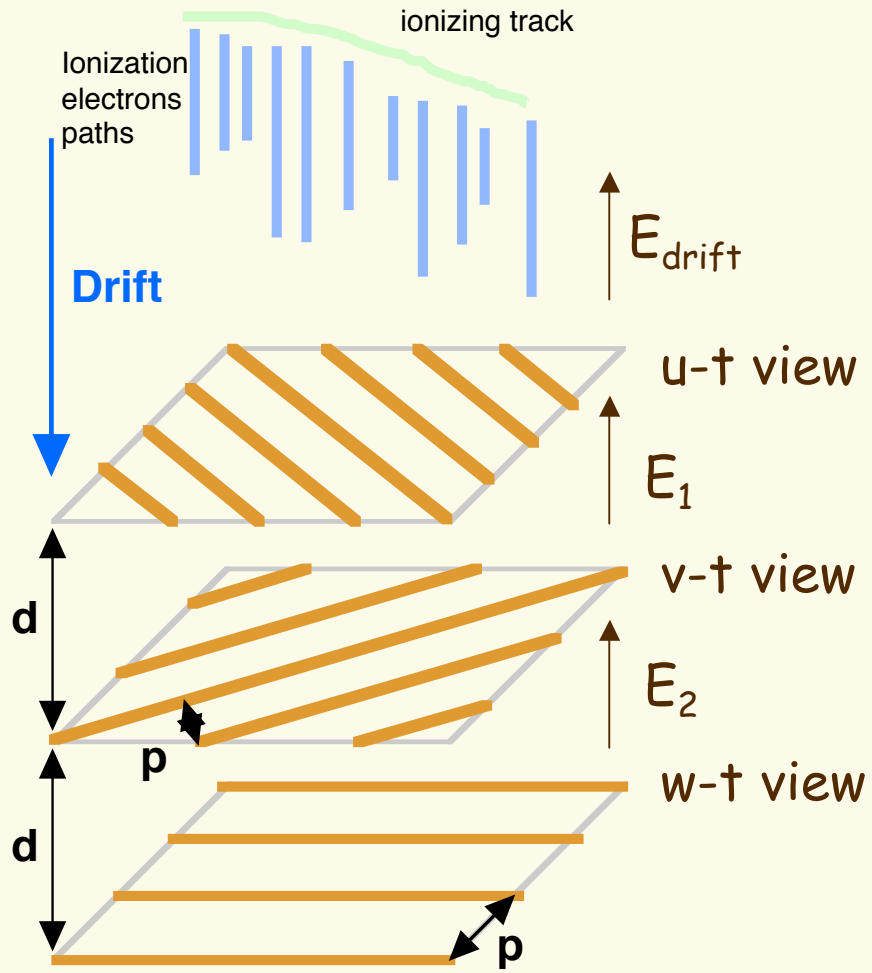
$$dW = E\, e\, (v_+ + v_-)\, dt = V_0\, i_0\, dt$$

$$i_0 = e\, (v_+ + v_-) / d \sim e\, v_- / d \qquad (v_- \gg v_+)$$

$$Q(x) = \int i_0\, dt = e\, (d - x) / d$$

- i_0 starts as soon as the event occurs
- space resolution given by the size of the capacitor
- a charge outside the capacitor is not detected

The 3D imaging in Liquid Argon



- Yield ~ 6000 electrons / mm
- Grid transparency:

  $E_1/E_{drift} = E_2/E_1 > (1+\alpha)/(1-\alpha)$

  $\alpha = 2\pi r/p$ (r=wire radius)
- Wire-to-wire shielding:

  $\eta = 1+\log(\alpha)\ p/(2\pi d)$

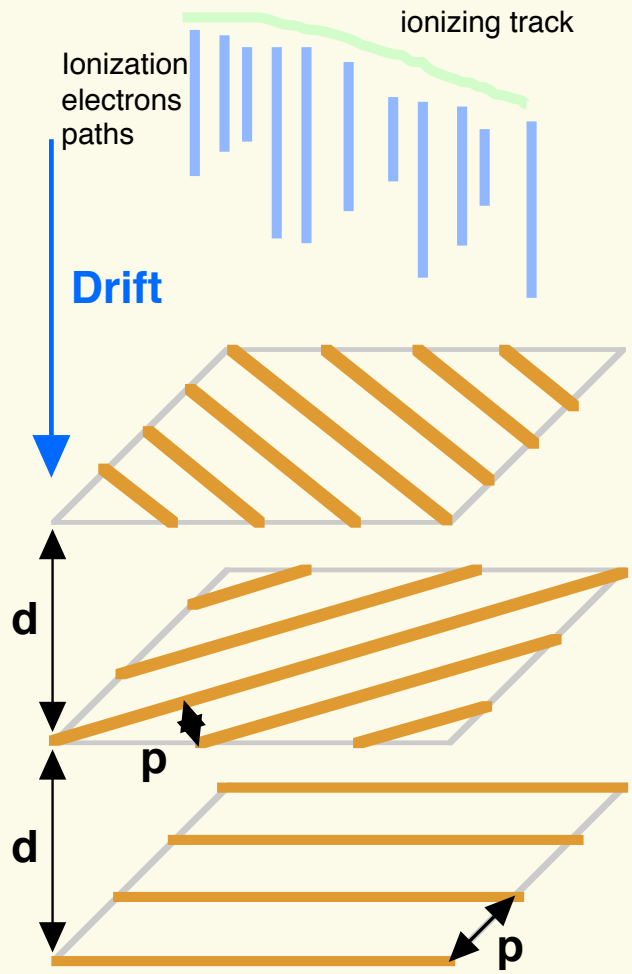
In the ICARUS LAr TPC

E_{drift} = 500 V/cm
p = 3mm
d = 3mm
r = 0.1mm

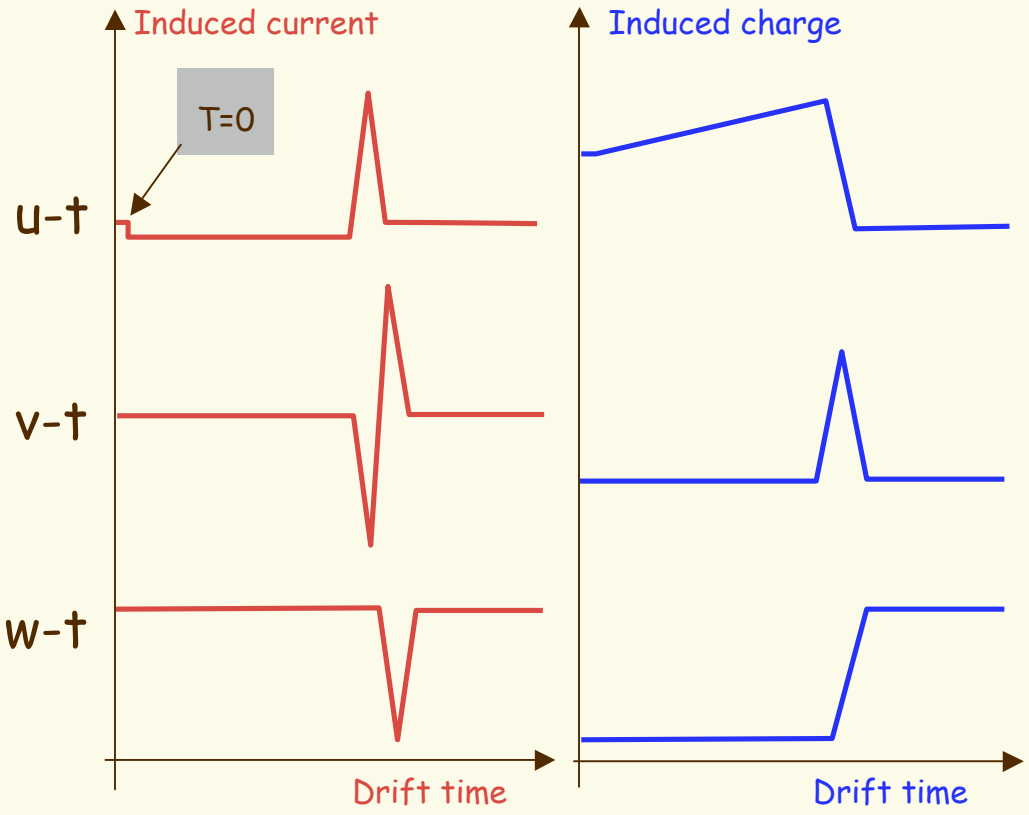
$E_1/E_{drift} = E_2/E_1 > 1.4$

$\alpha > 92\%$

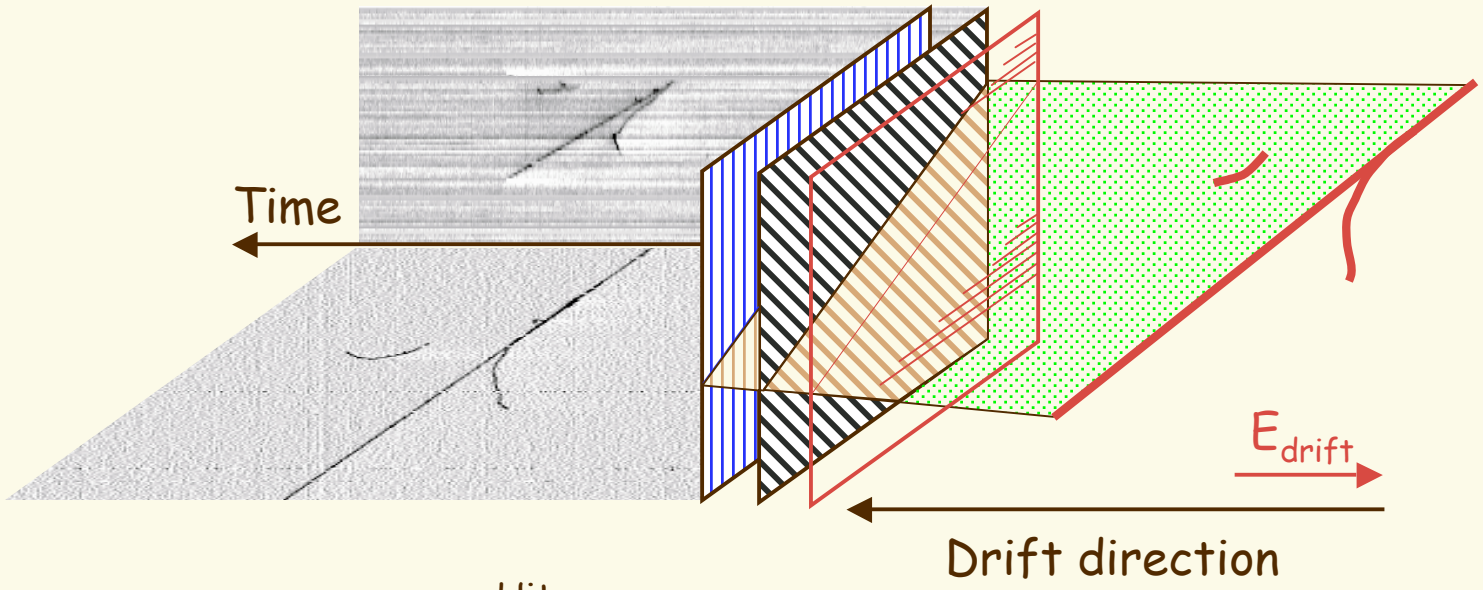
The induction signals

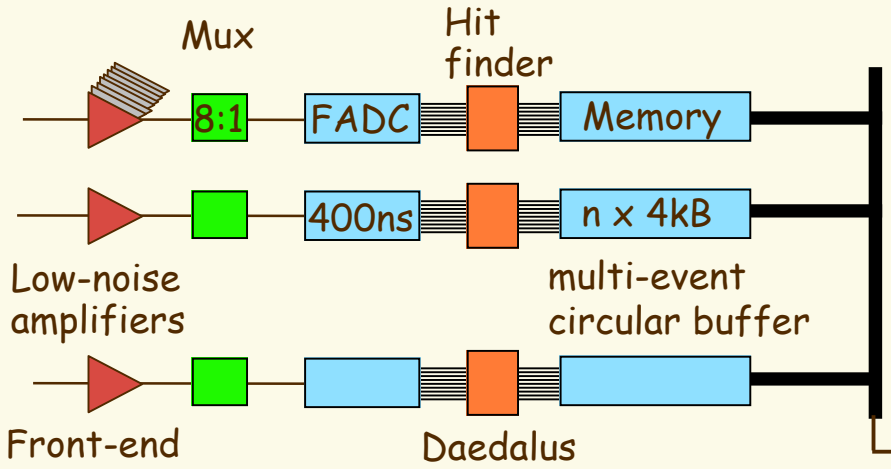


- Electron drift velocity ~ 1.5mm/□s
- Typical grid transit time ~ 2-3 □s



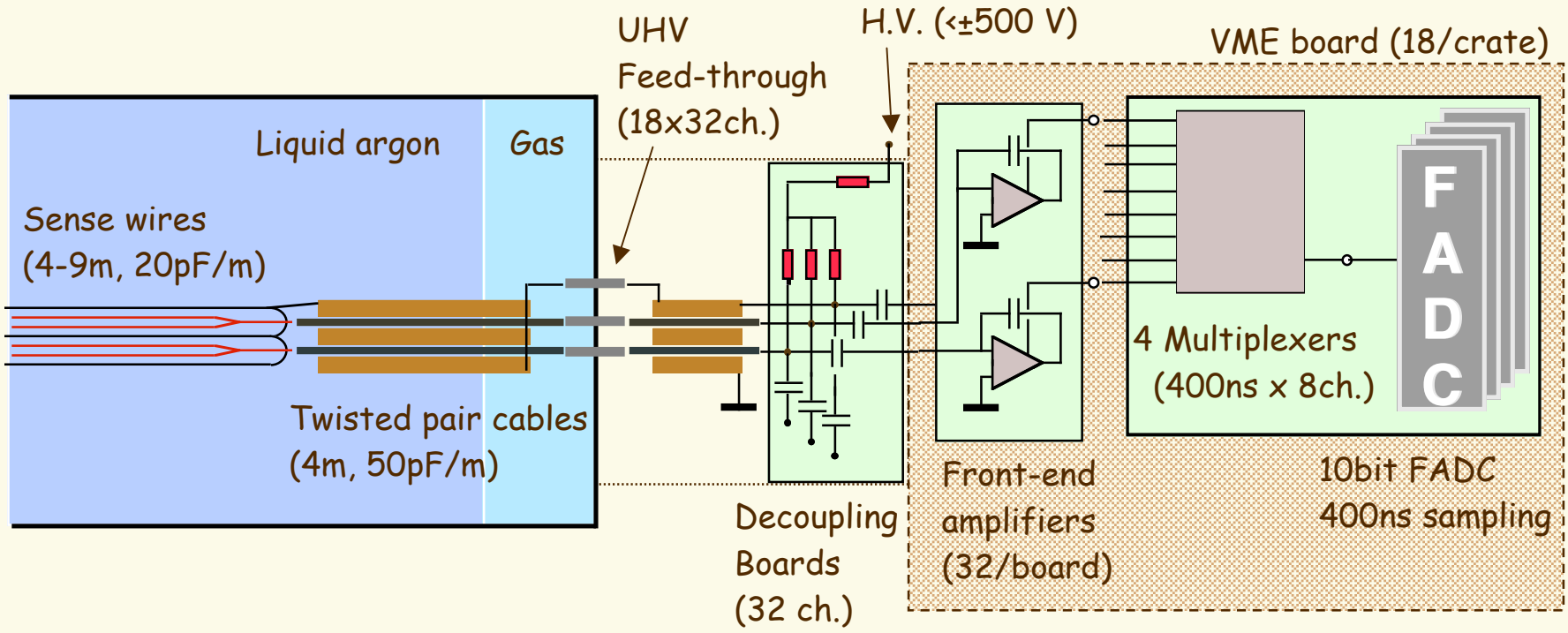
The ICARUS read-out principle





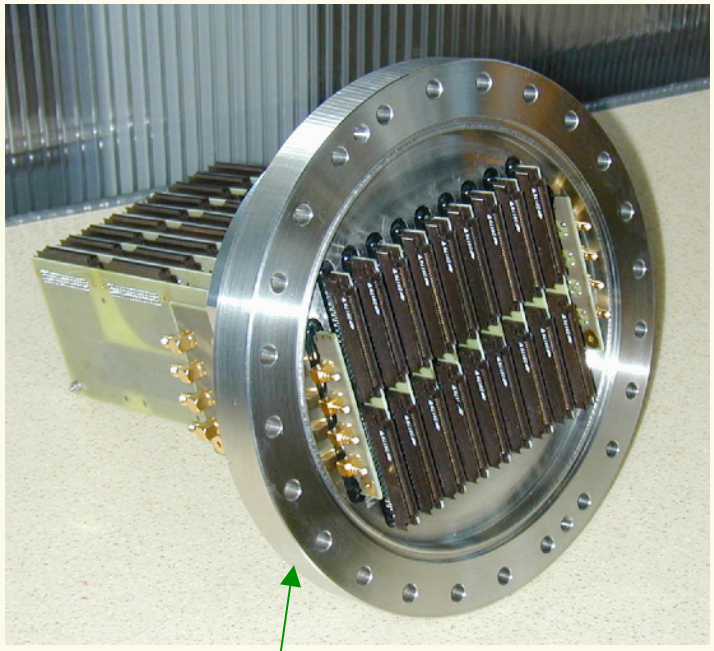
- Continously sensitive
- Self-triggering

Layout of front-end electronics



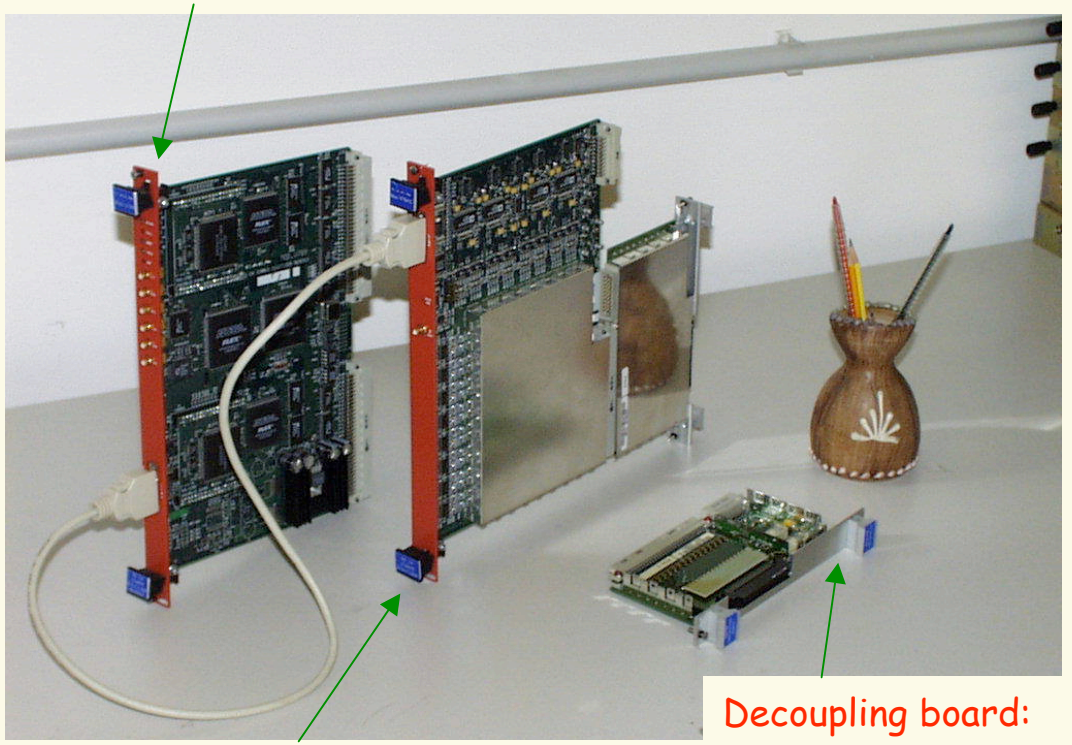
ICARUS T300: ~ 27000 channels — 860 boards — 48 crates

The ICARUS T600 read-out chain



Signal UHV feed-through:
576 channels (18 connectors x 32)
+ HV wire biasing

CAEN-V789 board: 2 Daedalus VLSI * 16 input channels (local self-trigger & zero suppression) + memory buffers + data out on VME bus

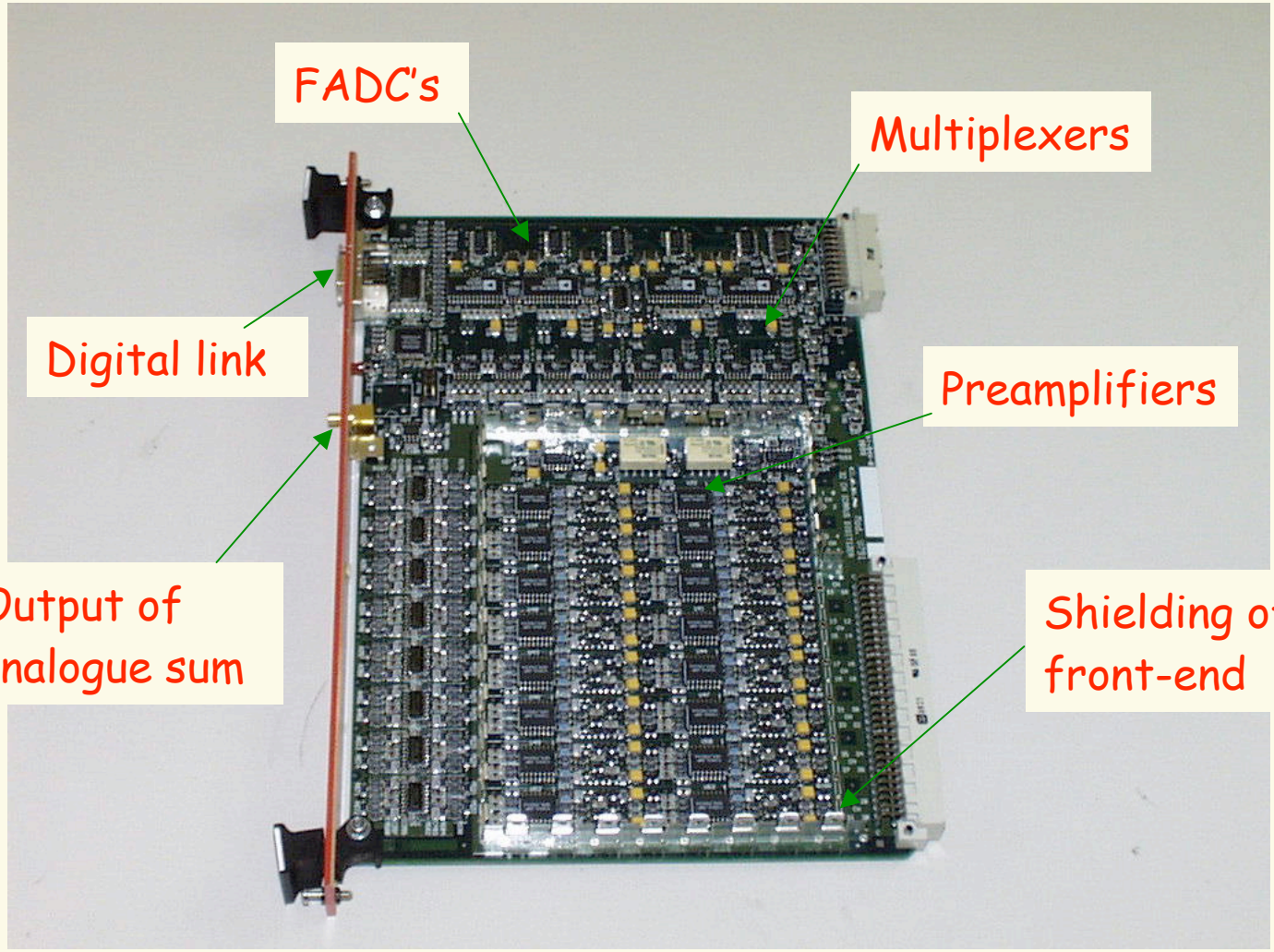


CAEN-V791 board: 32 pre-amplifiers +
4 multiplexers (8:1) + 4 FADC's (10 bits - 20 MHz)

Decoupling board:
HV distribution
and signal input

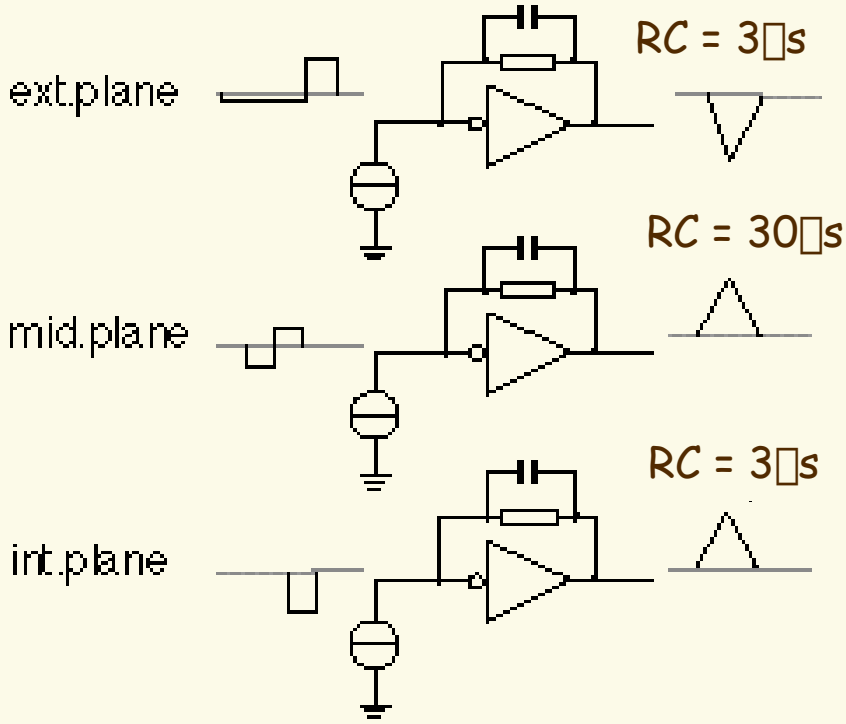
The T600 electronic racks

The analogue board CAEN-V791



Input signals & pre-amp feedback RC

- ✓ Ext. & Int. planes:
  - Approx. unipolar input signal
  - Width ≥ 3 μs
  - Short RC ("quasi-current" mode) to minimized pile-up
- ✓ Mid. Plane:
  - Bipolar signal
  - Long RC ("quasi-charge" mode) to get triangular signals

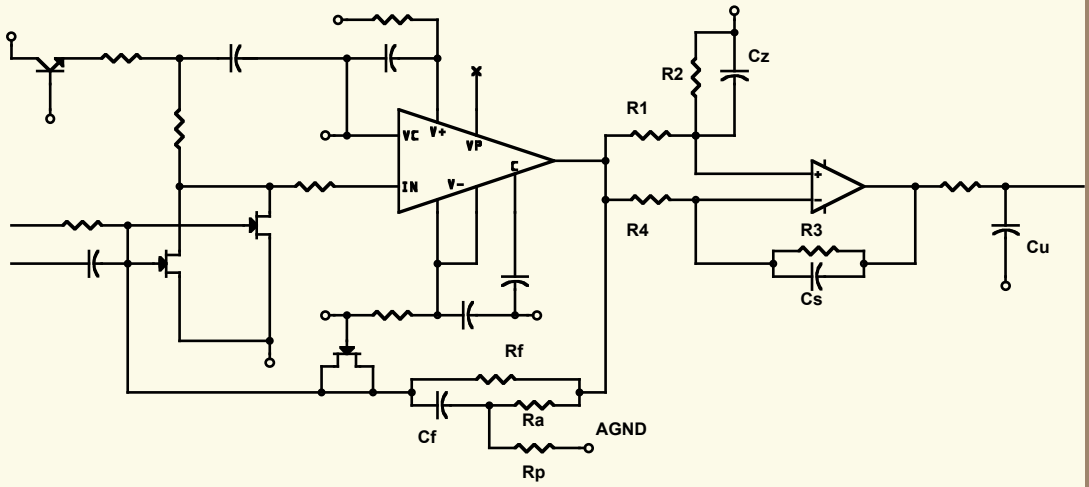


Expected signal: ~ 15000 electrons (3mm m.i.p.)

Equiv. Noise charge: (350 + 2.5 x C_{in}) electrons = 1200 el.

Optimization of the Analogue boards

- ✓ Goals (V791C & V791 Q):
  - Signal P.H. ~ 12 ADC for 3 mm m.ip.
  - Noise r.m.s ~ 1 ADC
  - FWHM ~ 5 μs
- ✓ Action on:
  - feedback RC
  - Gain and bandwidth of "baseline restorer"



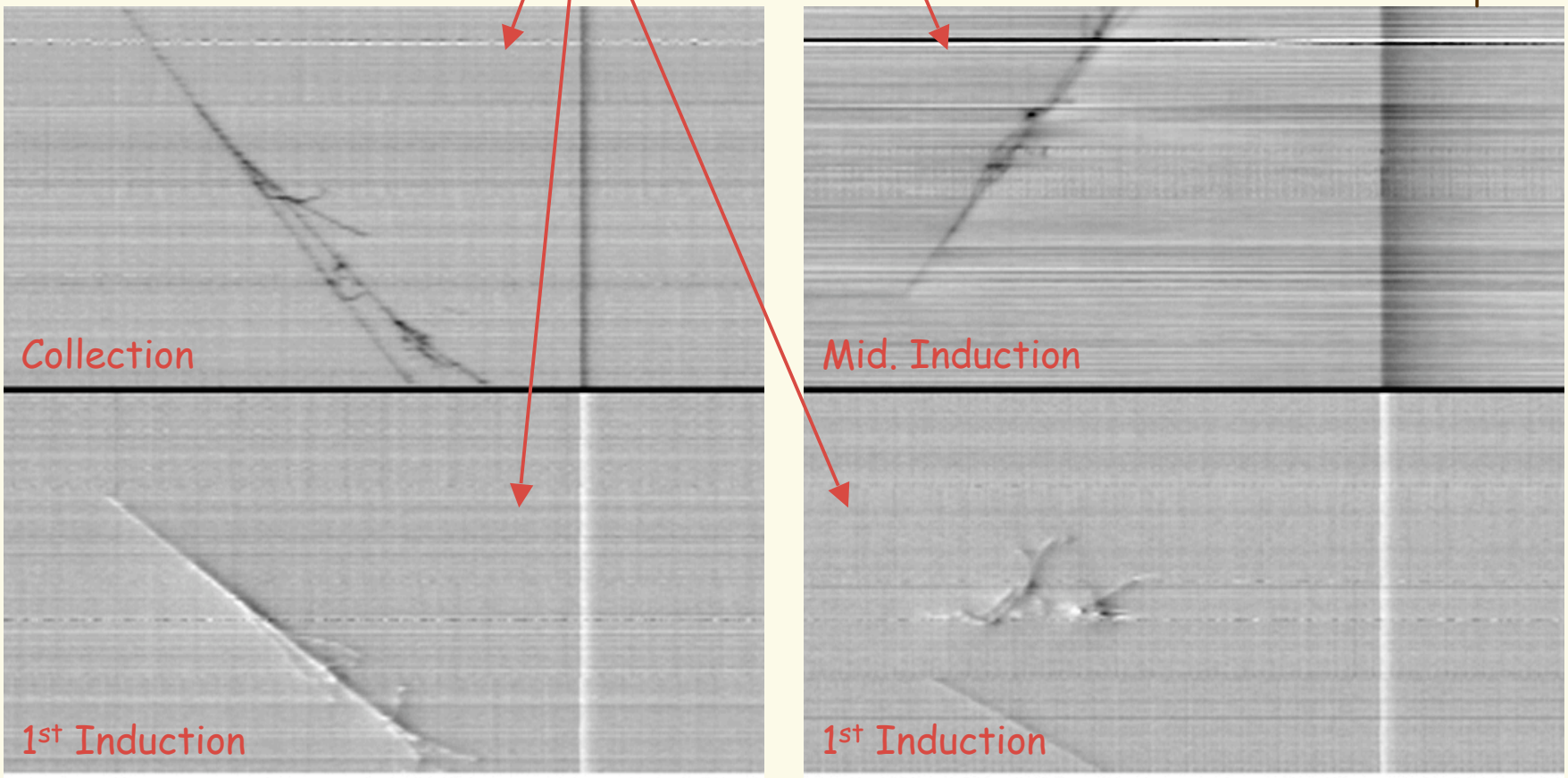
- ✓ Results:

Model	Rf	Cf	Rp	Ra	R1	R2	R3	R4	Cs	Cu	Cz
V791C	10 M□	3.3 pF ±10%	1.2 k□	22 k□	100 k□	270 k□	27 k□	10 k□	39 pF	2.2 nF	1 □F
V791Q	100 M□	1 pF ±10%	□	0 □	33 k□	270 k□	270 k□	33 k□	3.9 pF	2.2 nF	1 nF

Overall decay time constants: ~3μs (V791C) , ~30μs (V791Q)

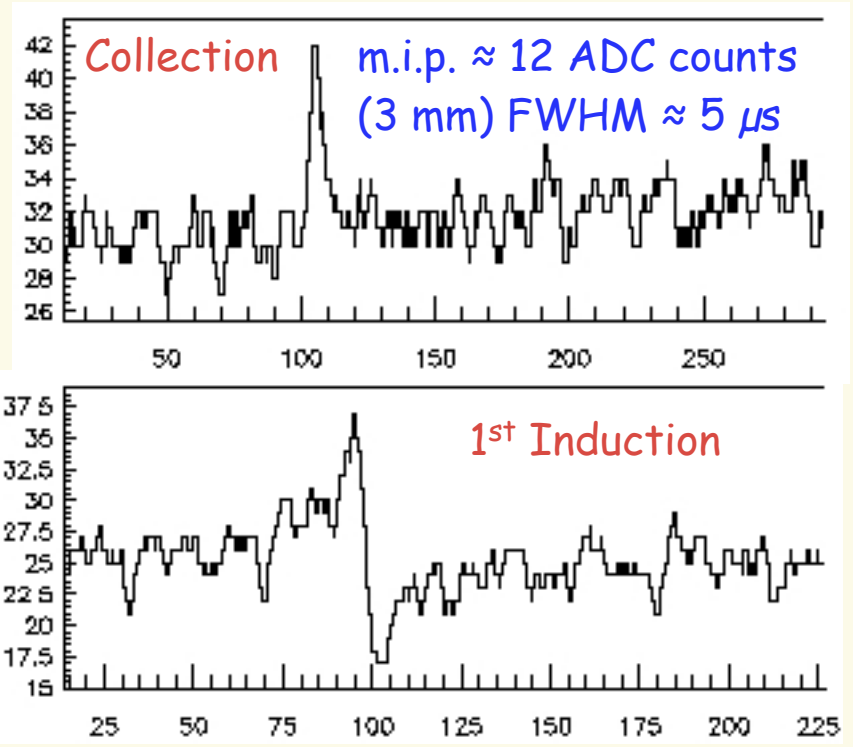
Performance of the V791 boards

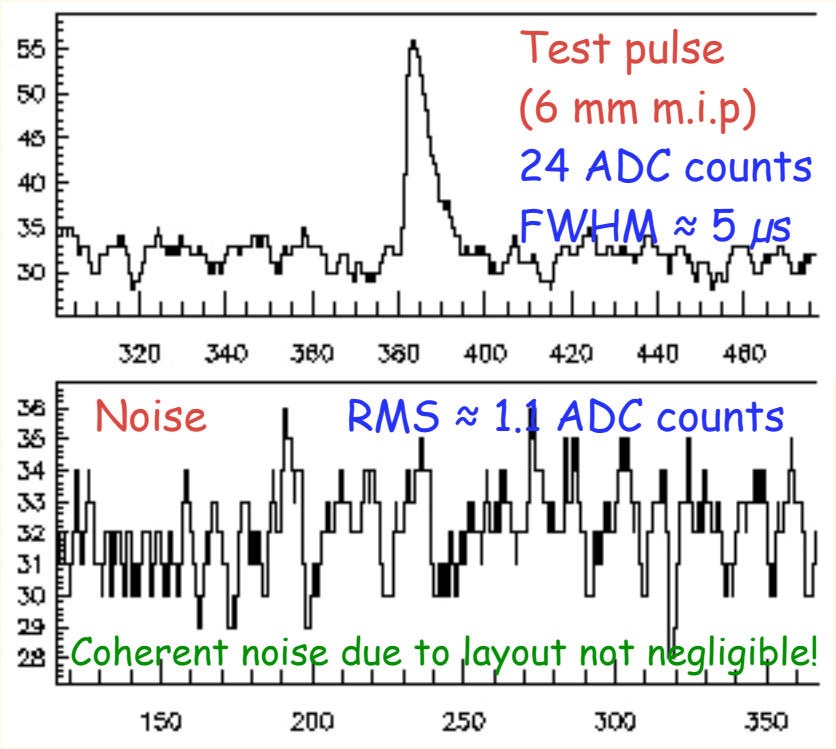
- ✓ Events (with PMT global trigger)



Performance of the V791C boards

- ✓ Single wire waveforms (horiz. axis unit = 400 ns)

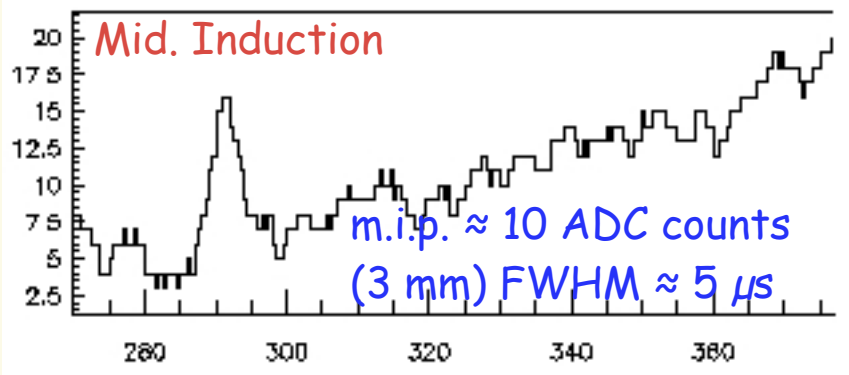


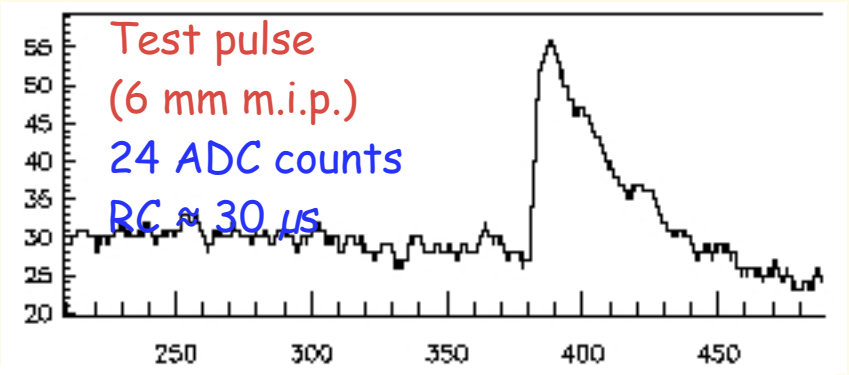


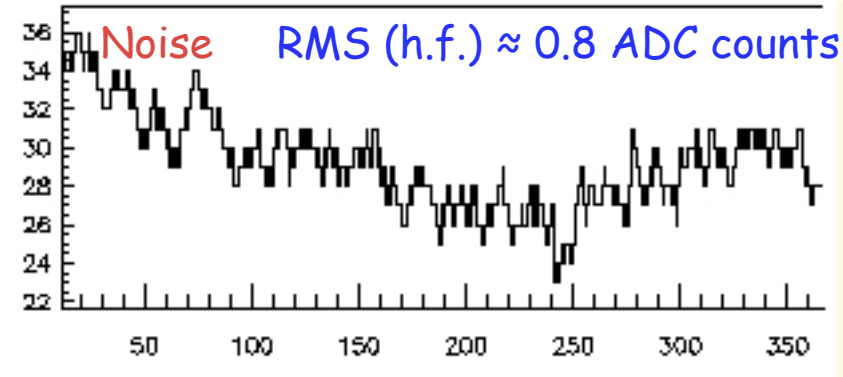
- ✓ RMS noise on T600 = 1.7 ADC counts (due to difficult environment in Pavia)

Performance of the V791Q boards

- ✓ Single wire waveforms (horiz. axis unit = 400 ns)



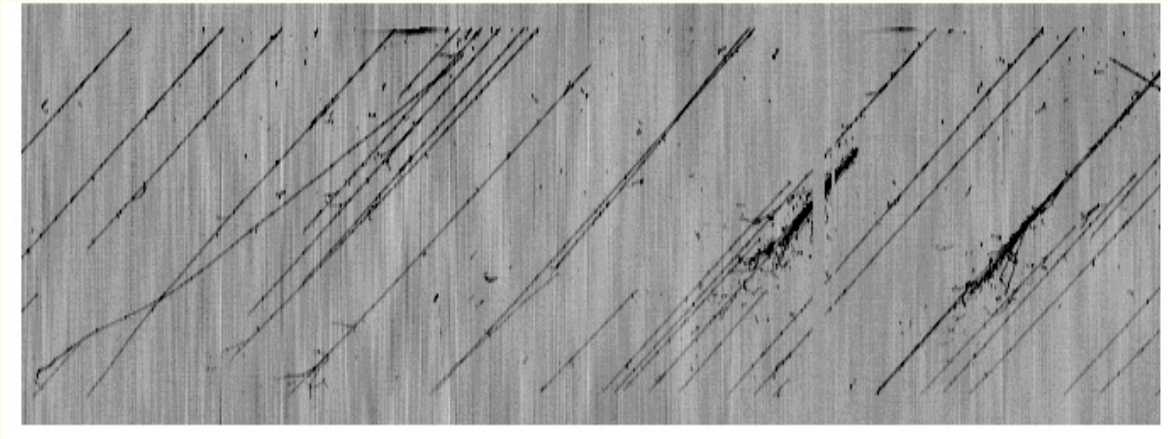




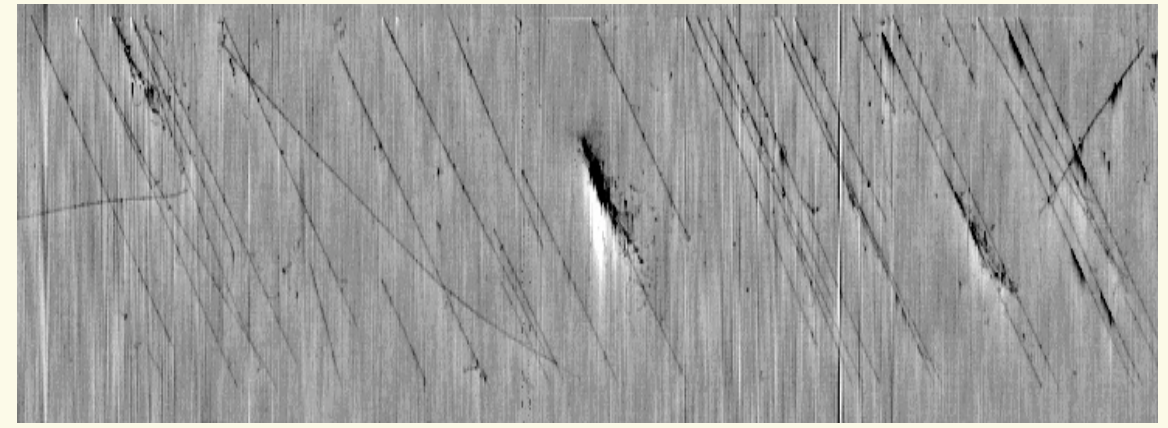
- ✓ Pulse height & shape from mid. plane wires very similar to those from collection plane wires.
- ✓ High frequency S/N also comparable.
- ✓ Low frequency minimized by shaper.

Low frequency noise visible but not dangerous! h.f. noise on T600 = 1.5 ADC counts

Events from the T600 semi-module

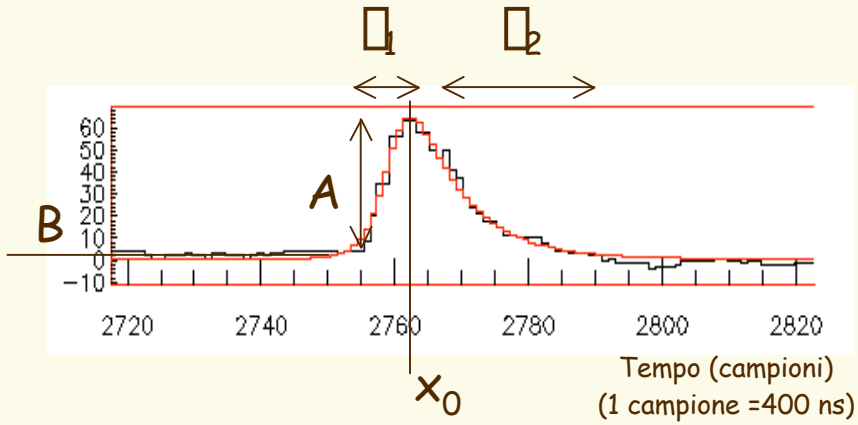


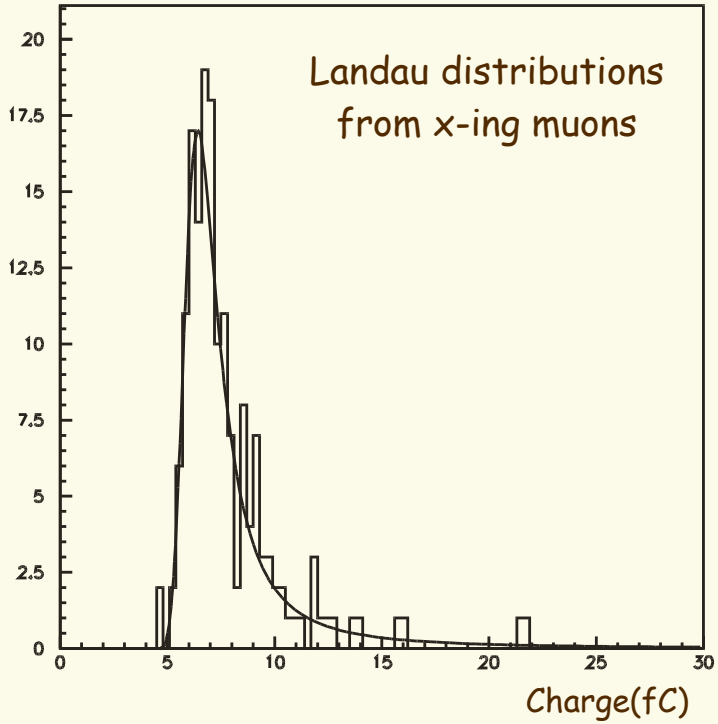
Collection view



Induction2 view

Event reconstruction

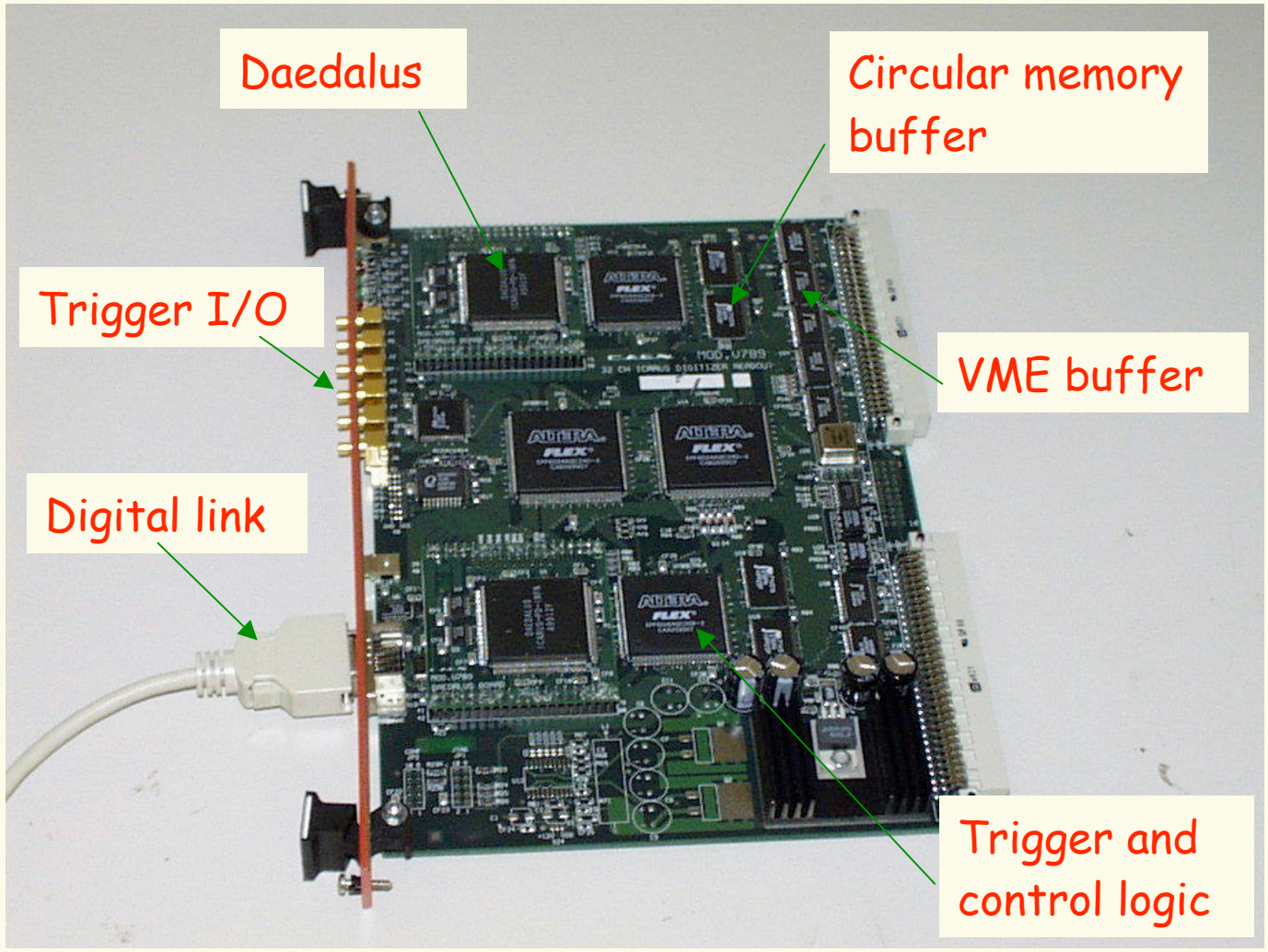




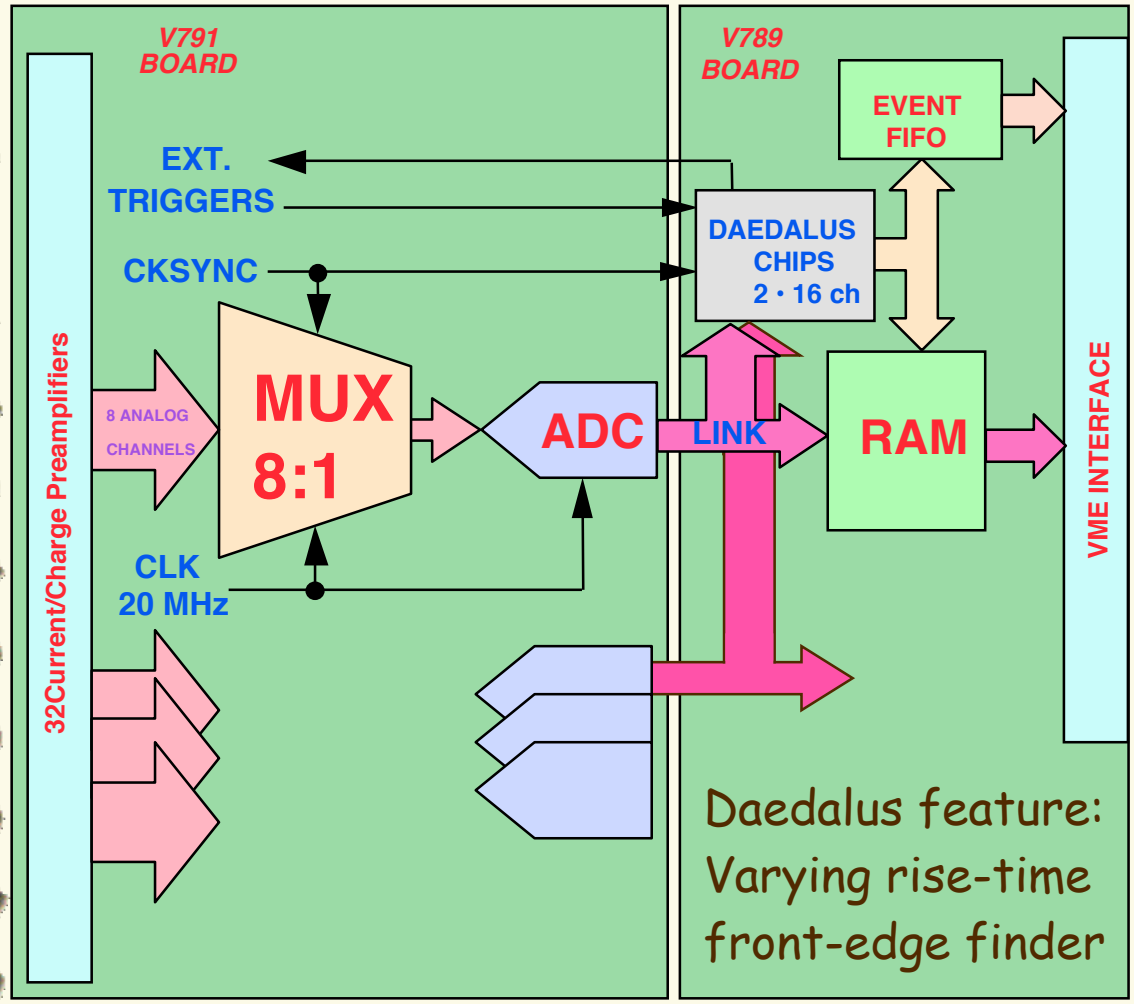
- ✓ Signal fit:
  - B = baseline
  - A = amplitude
  - τ_1 = risetime
  - τ_2 = falltime
  - x_0 = peak position

- ✓ Landau parameters (dE/dx, ξ) in agreement with expectation after:
  - Test pulse energy calibration
  - Free electron lifetime correction

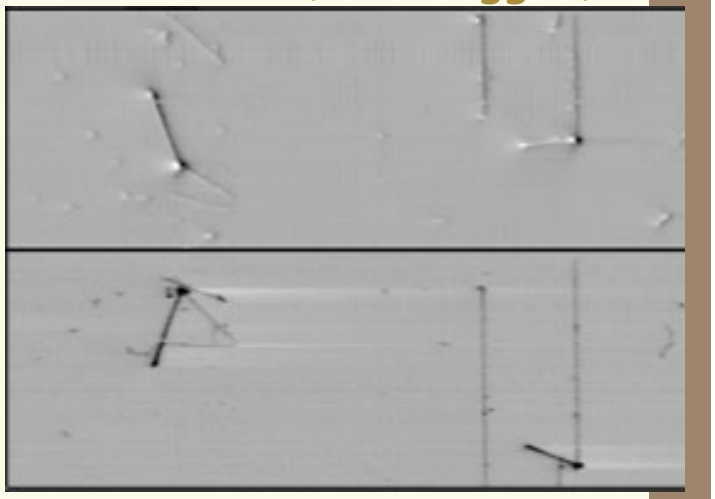
The digital board CAEN-V789



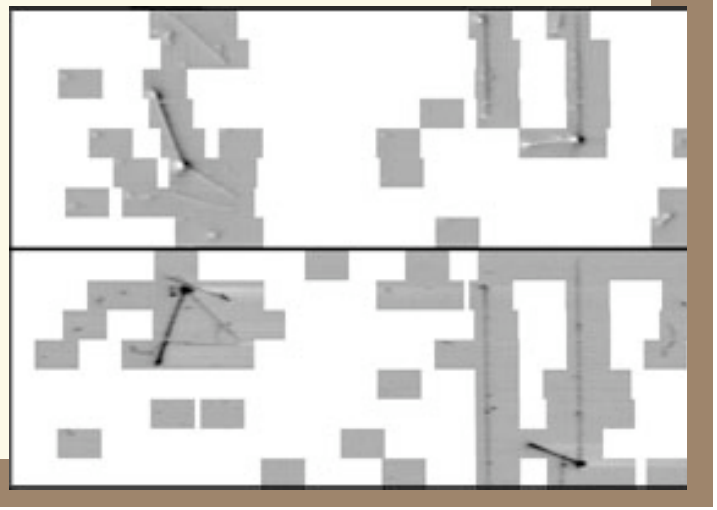
DAEDALUS: on-line zero suppressor and local trigger enabler



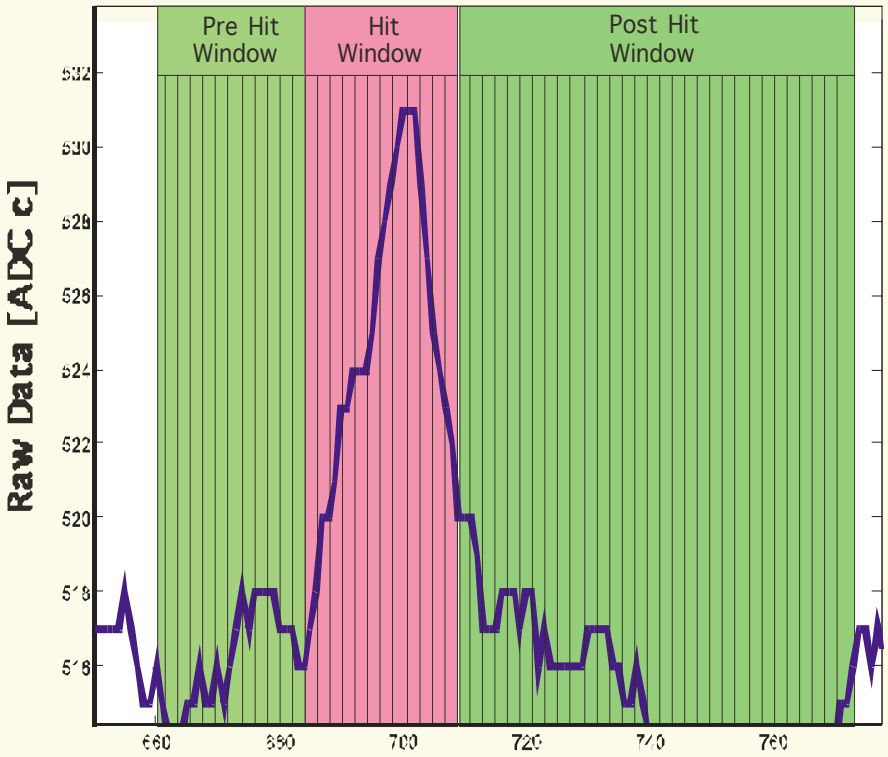
Raw data (ext. trigger)



Reduced data



Zero-Suppression Algorithm
Hitfinder + TileBuilding



Daedalus:
detects signal Rising-Edge, Falling-Edge, Width…
and generates a hitfound signal

TriggerLogic:
handles a 16 channels group
and builds a data tile around the hit

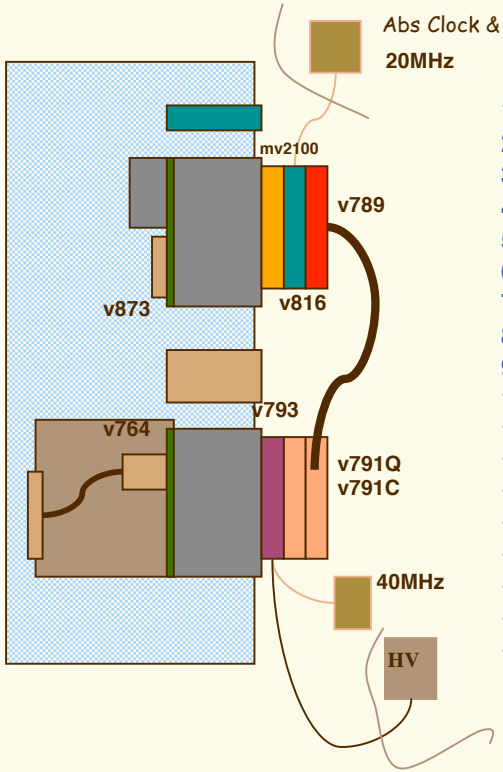
Present Performance on T300 RawData:
Efficiency= 97% Collection
90% Induction 1 & 2
False Detections= 20%

Studies underway for improvement of algorithm (promising…)

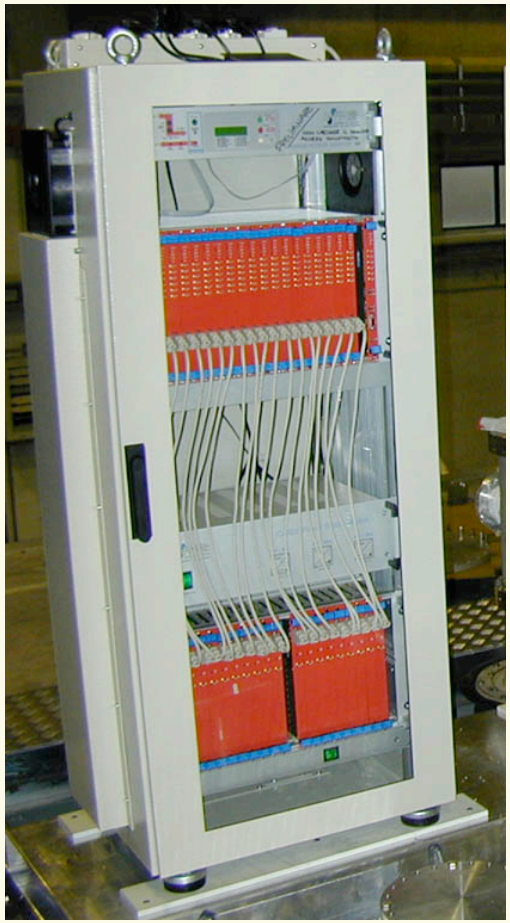
Event builder operating modes

- ✓ External trigger: PMT Analog OR + Full Drift Imaging
  - Limited in bandwidth (≈1 Hz max rate for 1.5 ms drift). Maximum of two events pile-up before deadtime.
- ✓ External Enable: PMT Analog OR + Daedalus hit finding
  - Bandwidth allows up to 1k event "tiles" (25 μs • 16 wires) per second per readout crate. Daedalus thresholds can be more tolerant without over-flooding readout.
  - Internal FIFO's can accept up to 128 fragments.
- ✓ Open Shutter: Daedalus hit finding
  - Same bandwidth as above. Useful to collect low energy events.
  - Drawback is that correlated noise bursts even at low repetition rate (few per second) would easily saturate the DAQ channel.

DAQ Read-out Rack



1 Flanges
2 Cables & Conn.
3 Screening Boxes
4 Decoupl. Boards
5 An. Backplanes
6 An. Crates
7 An. Power Supply
8 Slow Control Mod.
9 Charge An. Boards
10 Current An. Boards
11 Dig. Link Cables
12 Dig. Boards
13 Abs. Clock Trig. Mod.
14 Cpu
15 Dig. Backplane
16 Dig. Crate + P.S.
17 P.S. Fan Temp. Controller
18 Rack



96 (+4 spares) units on the t600

Air tight structure (to reduce post installation servicing). Fan controlled air flow through the alu heat exchanger moderates internal temperature.
A custom unit allows remote probing and control of rack status via an I2C interface.

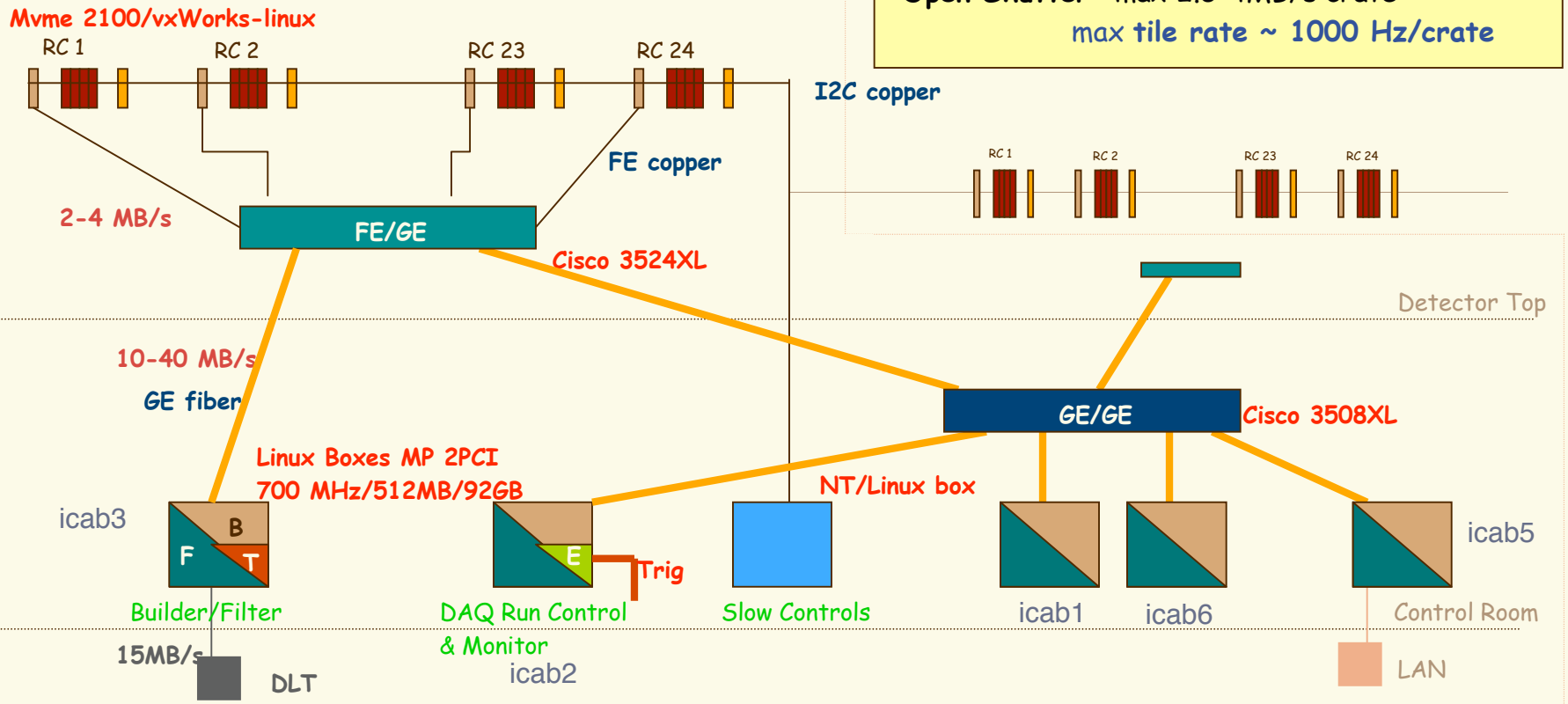
T600@PV DAQ layout

Readout rack interconnection is based on an fast ethernet/giga ethernet switched network. Event fragment merging load can be shared among a set of receivers.
One of the receivers also handles synchronization with trigger system.
An I2C bus is used for rack remote control.

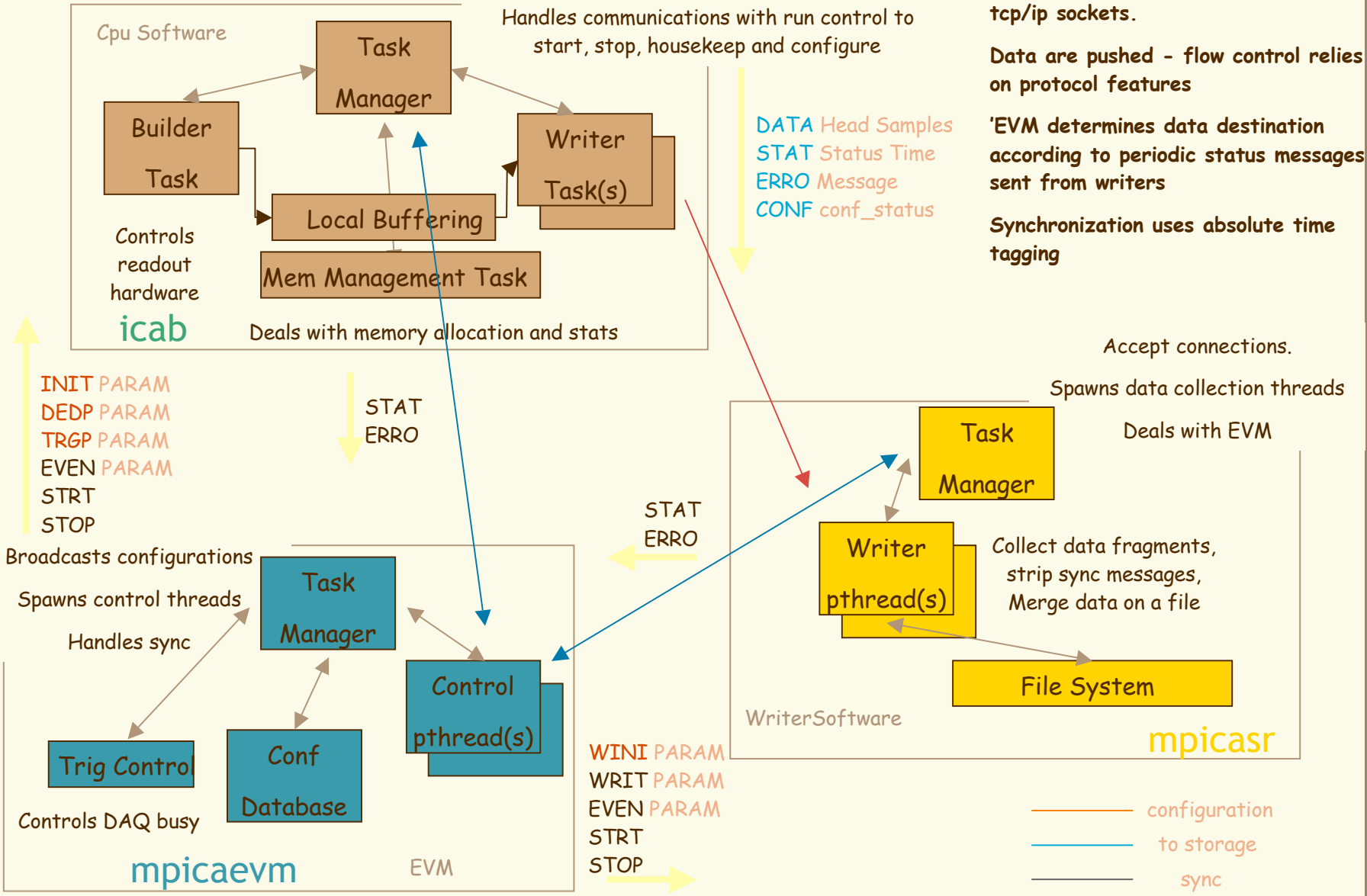
Full Imaging Mode :
2 * ~114 MB/ev ~.1 Hz

Daedalus Zero Skipping :
estimated 2 * ~.5-10 MB/ev 1-100 Hz

Open Shutter : max 2.5-4MB/s crate
max **tile rate ~ 1000 Hz/crate**



T600 Builder Overview



Lossless Compression Scheme

Sample n

16 bits

32 bytes

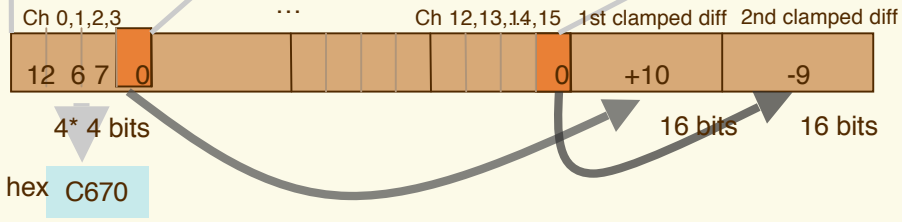
Sample n+1

16 bits

Difference n

16 bits

Achieved compression ratio on t600 data files ~ 3.9



Encoded Data

Sn+1 - Sn +8 if -8< diffn<8

0 else

Actual value (16 bits) follows for every clamped difference

12 bytes

Each sample is coded on 4 bits as the difference between itself and the previous sample (throwing the 6 bits carrying daedalus output). Should the difference be outside 4-bit boundaries (< 1% of samples), a flag is raised and the full 16 bits value is then used.