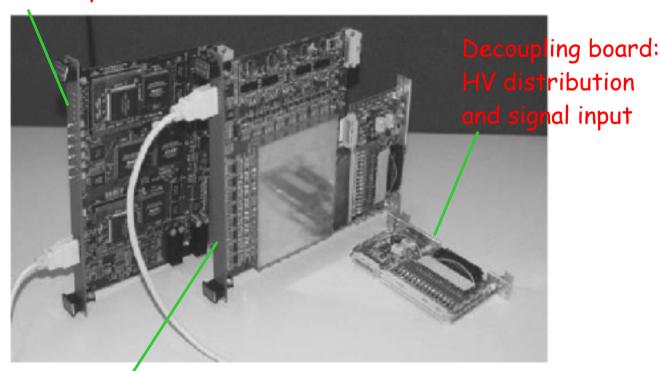
The new ICARUS read-out system Test results with the 50 | LAr-TPC

- ✓ Optimization on real data of S/N and shapes for the three different wire signals.
- ✓ Comparison of "all-out" with "preamp-in" front-end configurations.
- √ T=0 signal from scintillation as trigger enabler.
- ✓ Study of self triggering and zero-suppression with Daedalus.
- ✓ Tuning of DAQ software, on-line display and monitoring.

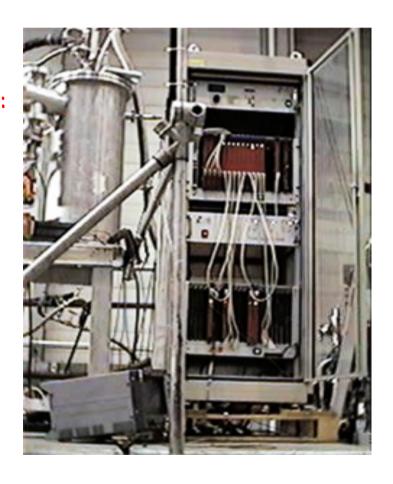
The ICARUS T-600 read-out chain

CAEN-V789 board: 2 Daedalus VLSI * 16 input channels (local self-trigger & zero suppression) + memory buffers + data out on VME bus



CAEN-V791 board: 32 pre-amplifiers + 4 multiplexers (8:1) + 4 FADC's (10 bits - 20 MHz)

One rack fully tested and optimized with real on-line data from the 50 liter Lar TPC



Test set-up with the 50 | LAr-TPC

- ✓ One complete rack shipped to CERN.
 - Housing the Analogue boards (V791C, V791Q), the Digital boards (V789 and V816), the Decoupling boards (DB), Power supplies and Control units.
 - Fully tested and validated in Padova. Serving 576 channels (18 boards 32 channels per board).
- ✓ Conditions as close as possible to final layout of T-600.
 - Three-wire-plane configuration (total read-out channel = 256).
 - Electric field in drift volume: 500 V/cm.
 - T600 feed-through.
 - \approx 180 pF input capacit. (2 m of T600 cables + connectors + wires in LAr).
 - HV distributed on wires from decoupling boards through cables.
 - One PMT (EMI 9426) for Ar scintillation placed in gas phase for T=0.

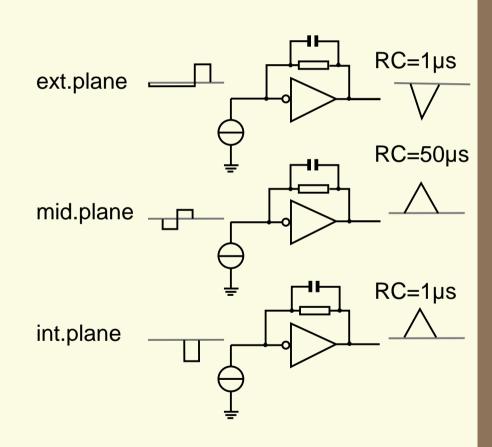
Input signals & pre-amp feedback RC

✓ Ext. & Int. planes:

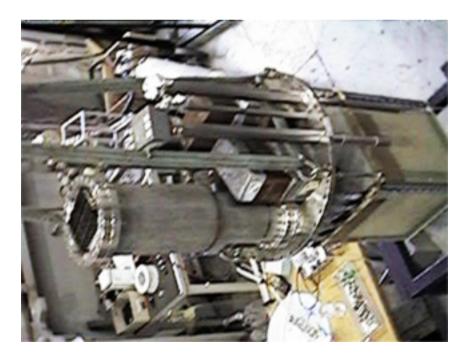
- Approx. unipolar input signal
- Width ≥ 3 µs
- Short RC
 ("quasi-current" mode) to
 minimized pile-up

✓ Mid. Plane:

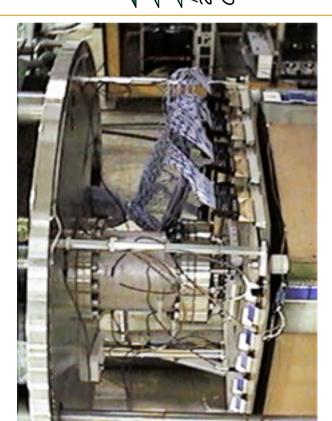
- Bipolar signal
- Long RC
 ("quasi-charge" mode) to get
 triangular signals



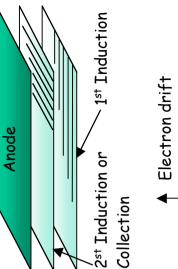
The 50 liter LAr-TPC







Read-out electrodes configuration



direction

Cathode

Optimization of the Analogue boards

✓ Goals (V791C & V791 Q):

- Signal P.H. ≈ 12 ADC for 3 mm m.ip.
- Noise r.m.s ≈ 1 ADC
- FWHM ≈ 5 μs

✓ Action on:

- feedback RC
- Shaper gain and bandwidth

mm m.ip.

✓ Results:

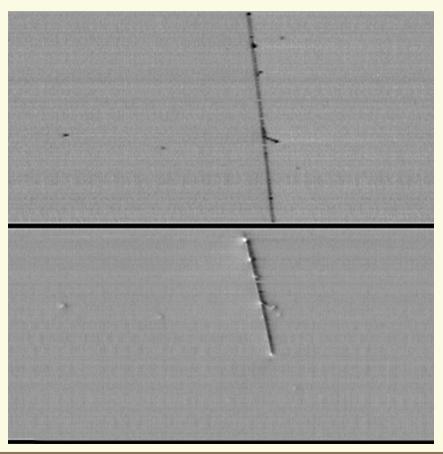
Model	Rf	Cf	Rp	Ra	R1	R2	R3	R4	Cs	Cu	Cz
V791C	10 M Ω	3.3 pF ±10%	1.2 k Ω	22 k Ω	100 k Ω	270 k Ω	27 k Ω	10 k Ω	39 pF	2.2 nF	1 μ F
V791Q	100 M Ω	1 pF ±10%	$\infty \Omega$	0 Ω	33 k Ω	270 k Ω	270 k Ω	33 k Ω	3.9 pF	2.2 nF	1 nF

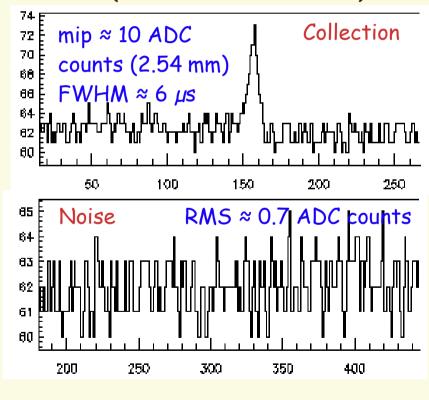
Overall decay time constants: \approx 3 μs (V791C), \approx 40 μs (V791Q)

Events with old electronics

Preamplifiers in liquid Argon (very low input capacitance)

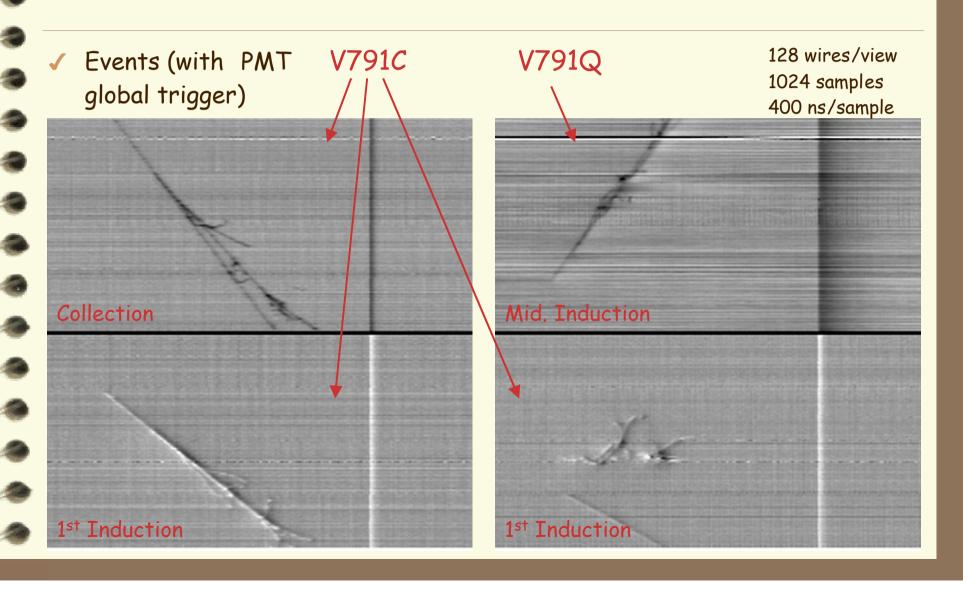
(horiz. axis unit = 800 ns)





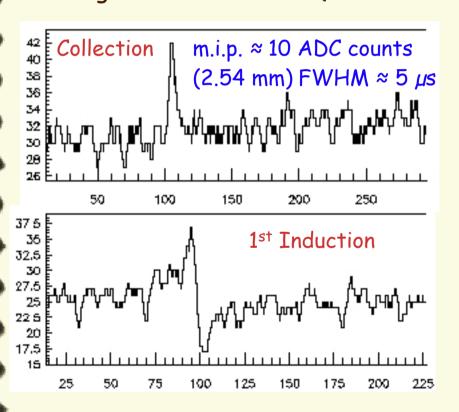
Negligible coherent noise!

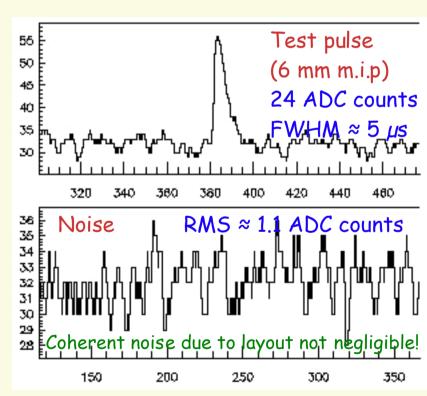
Performance of the V791 boards



Performance of the V791C boards

✓ Single wire waveforms (horiz. axis unit = 800 ns)

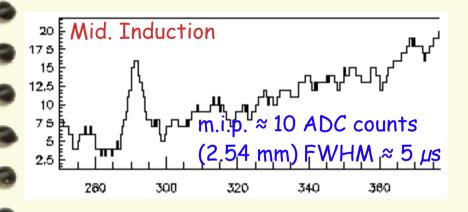




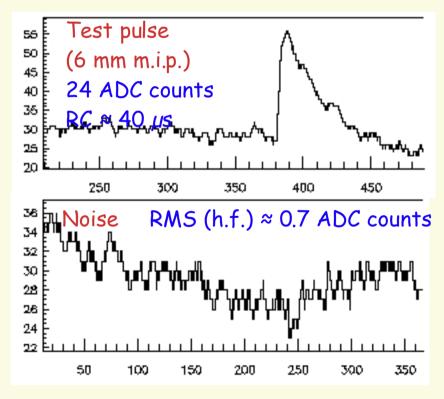
✓ Very similar to old electronics except for residual coherent noise!

Performance of the V791Q boards

✓ Single wire waveforms (horiz. axis unit = 800 ns)



- ✓ Pulse height & shape from mid. plane wires very similar to those from collection plane wires.
- ✓ High frecuency S/N also comparable.
- ✓ Low frequency minimised by shaper.



Low frequency noise visible but not dangerous!

Recording the PMT prompt signal

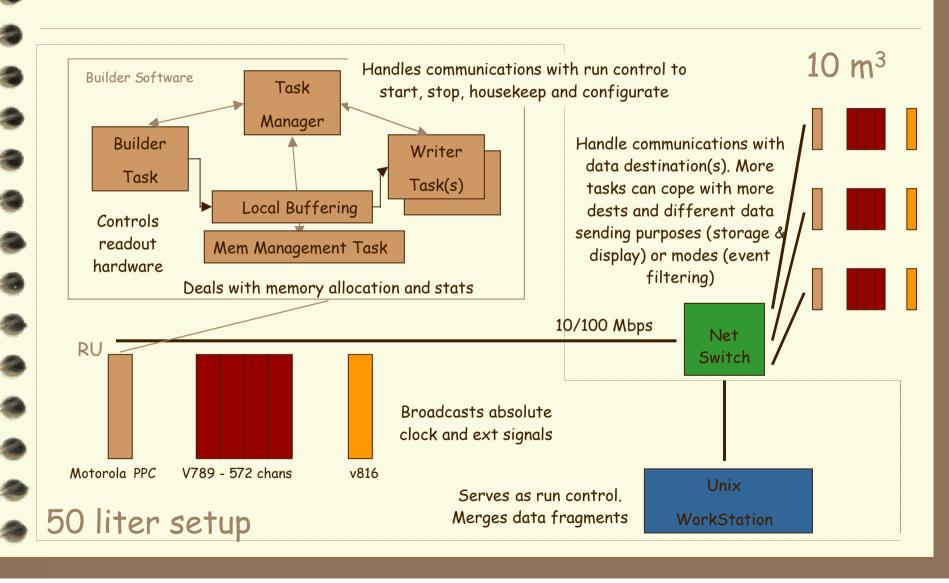
✓ PMT Characteristics:

- EMI 9426 with MgF_2 window (ϕ =2 inches)
- Q.E. (@ 128 nm) ≈ 20-25 %
- Gain (@ 1380 V) ≈ 10⁶
- Tipical m.i.p. signal: tens of photoelectrons
- Signal width ≈ 30 ns (base)
- Housed in evacuated case with MgF₂ window (located in Ar gas phase)

✓ Use:

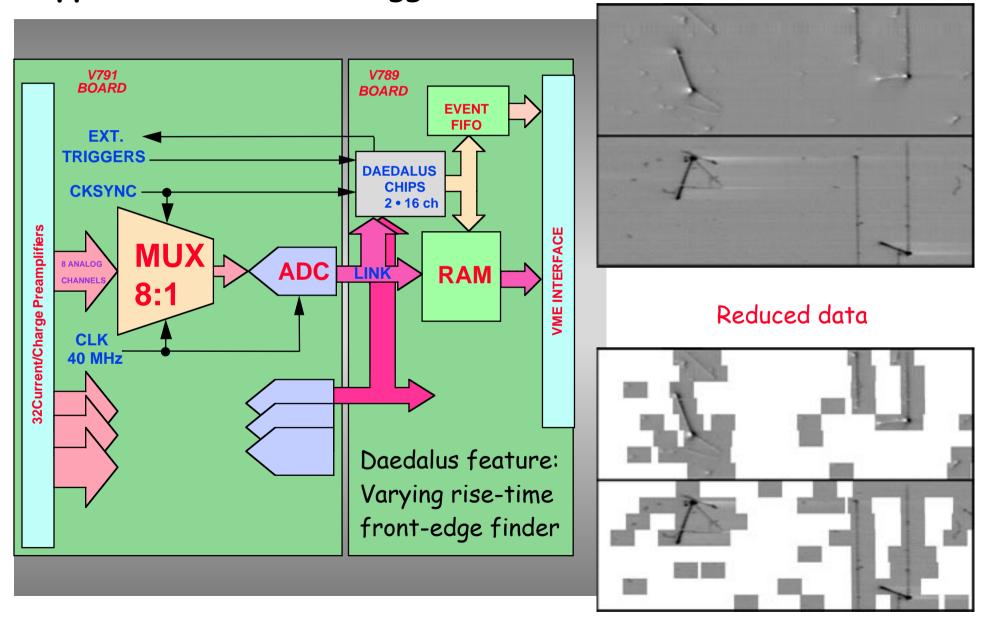
- Global external trigger
- Internal trigger enabler
- Recorded with a modified version of the V791Q board:
 - Pre-amp sensitivity:
 1 pC = 25 mV
 Decay time ≈ 400 μs
 - No multiplexer:
 50 ns sampling time
 - 4 channels per board
 - Muon signal in the 50 | LAr-TPC
 > 50 mV

Present DAQ structure



Daedalus chip as on-line zero suppressor and local trigger enabler

Raw data (ext. trigger)



Event builder operating modes

- ✓ External trigger: PMT

 Analog OR + Full Drift Imaging
 - Like the old Icarus readout. Limited in bandwidth (≈1 Hz max rate for 1.5 ms drift). Maximum of two events pile-up before deadtime.
- ✓ External Enable: PMT

 Analog OR + Daedalus hit finding
 - Bandwidth allows up to 1k event "tiles" (25 μ s · 16 wires) per second per readout crate. Daedalus thresholds can be more tolerant without overflooding readout.
 - Internal FIFO's can accept up to 128 fragments.
- ✓ Open Shutter: Daedalus hit finding
 - Same bandwidth as above. Useful to collect low energy events.
 - Drawback is that correlated noise bursts even at low repetition rate (few per second) would easily saturate the DAQ channel.

DAQ status

✓ Ongoing tests:

- Prototype event builder tested on the 50 liter LAr-TPC. Event fragments forwarded via tcp/ip socket, also used for run control. Data streamed by pushing (no event requests) with the tcp/ip intrinsic flow control. Merging done at reception.
- Found serious problem with the absolute clock tagging, resulted inconsistent from board to board. Presently under investigation by Caen. Also affected Daedalus efficiency evaluation, since internal triggers cannot be correlated.
- Particular effort and time put in finding the correct layout for grounding (which results very detector and environment dependent), to minimize coherent noise level and reduce bursty pick-ups which would very quickly saturate internal triggering.
- On-line event display still under construction. A preliminary library handles the event reconstruction (temporary storage of fragments, handling of housekeeping tags which signals that all data for a given time window have been collected) and interfaces to off-line event display. Present data format to be integrated with further info for the off-line (run configuration, detector configuration, etc.).

DAQ status

✓ Readout hardware:

- Two racks already operational. Two more ready to be assembled.
- Under production:
 - Decoupling Board (postponed due to crosstalk problem now solved);
 - Modified versions of the V791 (C&Q) by CAEN, according to the new shaping configuration;
 - Slow Control Boards.
- Four CPU's and one 12 port 100 Mbps switch ready to be installed.

✓ Works in progress:

- One rack already installed and working on the 10 m³ at LNGS.
- DAQ campaign successfully started also on the $10\ m^3$.
- Next racks will follow upon receiving of DB's and V791's (\approx 2 months).
- Integration of several racks will put under spot the scalability issues of the system.
- The DAQ chain handles up to few Mbytes per second per crate (≈ 500 Daedalus "tiles" per second): a plan on how to organize the handling of the collected data is under study.