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Low-noise BiCMOS front-end and fast analogue multiplexer for ionization chamber

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Abstract

For Icarus detector a low-noise front-end amplifier, that works together with a 16 input analogue multiplexer, has been designed using AMS 0.8 μm BiCMOS technology. To achieve a suitable noise level of less than 1500 electrons with detector capacitance of about 400 pF, a high conductance JFET has been used as input device. The multiplexer works up to 40 MHz clock rate with 10 bit accuracy.

1. Introduction

Each 600 Ton Icarus TPC has three wire planes, with wire pitch of 3 mm, allowing three readout coordinates at 60° from each other. In total there are about 46 000 analog channels: 42 000 have wires 4 m long, 4000 have wires 9 m long. Wire length and connecting cables set the total input capacitance of the preamplifier (400 pF) and because of the high capacitance between adjacent wires the preamplifier input impedance should not exceed a few hundreds Ohms in order to minimize the wire cross talk. Charge signals, from a few fC to some tens fC, with minimum duration of about 1.5 μs, need to be detected and a signal-to-noise ratio of about 10 is required. Front-end electronics lies outside the dewar, working at room temperature, and consists of a charge preamplifier followed by a $\times 10$ single ended to differential driver and a 16 : 1 multiplexer that drastically reduces the number of channels needed for transferring data to the control room.

2. Preamplifiers

We have proposed two solutions as preamplifier architecture, both having common features:

- use of external high transconductance JFET as input device;
- external capacitor compensation for a suitable phase margin adjustment;
- external feedback network allows to use a 100 MΩ feedback resistor that reduces the parallel noise and allows to change the sensitivity;

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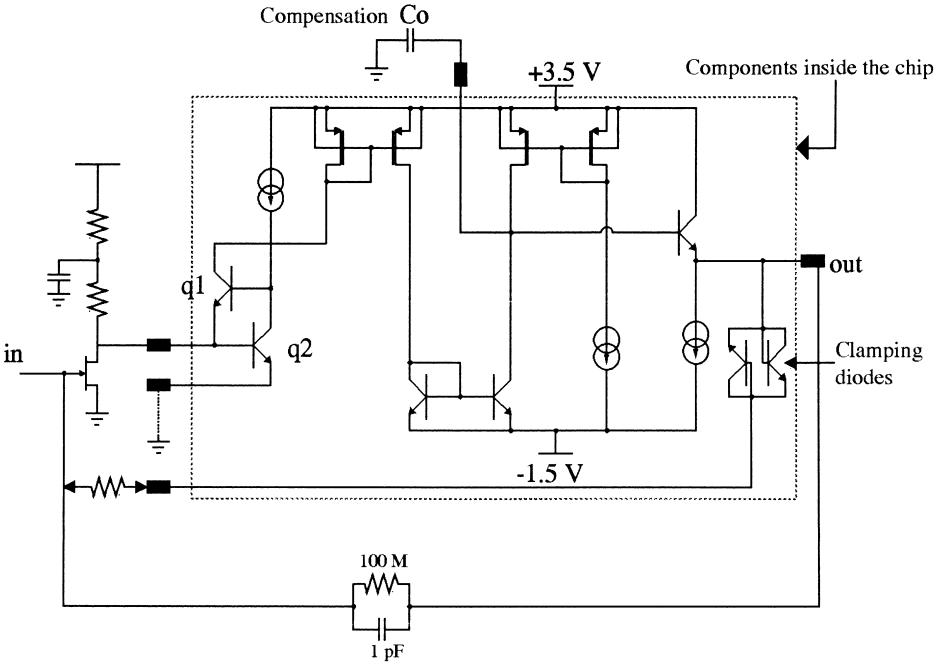

Fig. 1. CCA schematic.

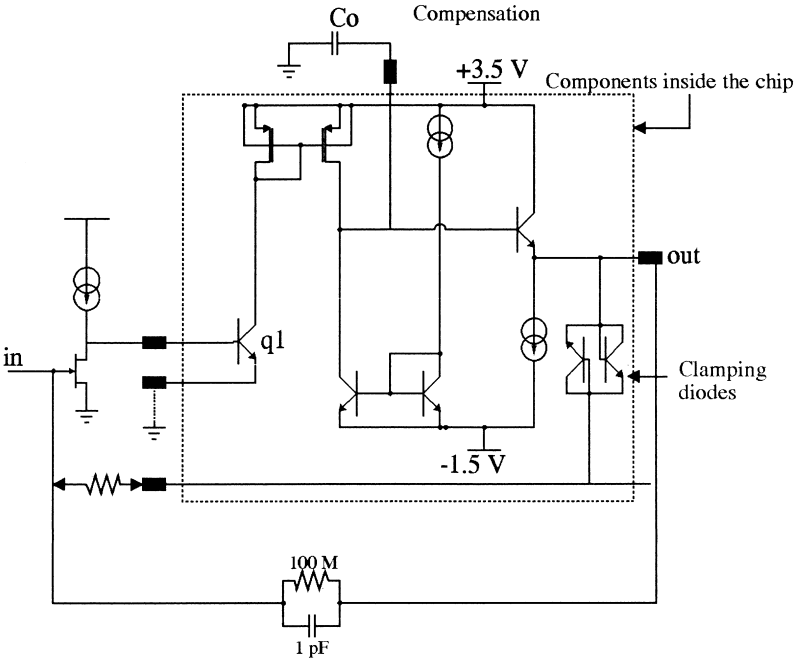

Fig. 2. TSCA schematic.

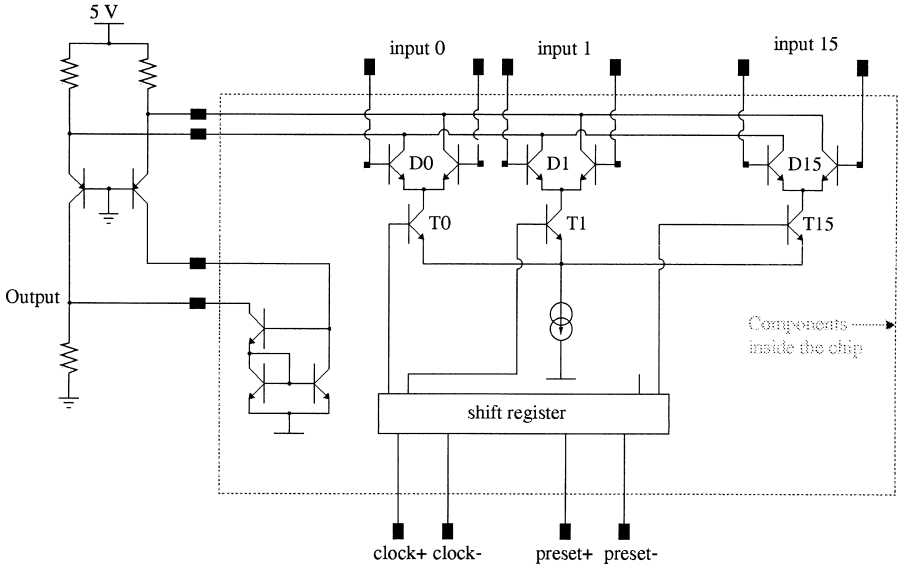

Fig. 3. Multiplexer schematic.

- high-input charge pulses can cause output saturation, so on-chip-clamping diodes can be connected to JFET gate through an external resistor to provide a fast recovery time.

Other common characteristics are the $+3.5$ V, -1.5 V dual voltage supply, the 1 mV/fC sensitivity and the 40 mW power consumption. Two discrete n-JFETs (2sk300 SONY) parallelly connected have been used providing a transconductance of about 40 mS. One preamplifier, called CCA (Charge Cascade Amplifier, Fig. 1), uses a Radeka configuration, while the TSCA (Two Stages Charge Amplifier, Fig. 2) basic amplifier is composed by a common source followed by a common emitter stage. The chip, $0.20 \times 0.27\,\text{mm}^2$, is housed in a 16 pin CSOIC package and at present is under test; preliminary results have shown satisfactory noise performance.

3. Multiplexer

The fast analog multiplexer (Fig. 3) works up to 40 MHz clock rate with 10 bit accuracy. Because for the on-chip logic only external clock and preset signal (that run at $\frac{1}{16}$ clock frequency) are needed. Digital signals are differential and logic levels of -0.8 and 0 V are used. Multiplexing operation starts after a preset signal; this helps to maintain a correct synchronization if a preset signal is sent every 16 clock periods. Differential analog inputs accept signals up to 1 V. The output is realized by an open collector–emitter-coupled pair and an external driver switch to single-ended output that allows a connection of a 50 Ω load. The circuit operates between -4.2 and $+0.8$ V and dissipate, driver included, about 170 mW. The $2.6 \times 2.3\,\text{mm}^2$ chip is housed in a 68 pin JLCC package and the prototypes are expected by the end of June.