The trigger system of the ICARUS experiment

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***Abstract*— This paper presents the hardware architecture and the main features of the ICARUS trigger system. The ICARUS detector is a very massive liquid Argon Time Projection Chamber aimed at the study of some of the fundamental issues of astroparticle physics such as solar and atmospheric neutrino interactions, neutrinos following a Supernova explosion, neutrino oscillations with beams from particle accelerator, nucleon decay for some channels predicted by GUTs. The main feature of the proposed trigger design is its "segmentation", i.e. the capability to trigger different sectors of the detector on different events allowing for the efficient detection of rare events.**

I. Introduction

The ICARUS (*I*maging *C*osmic *A*nd *R*are *U*nderground *S*ignal) detector is aimed at the study of a wide range of fundamental issues in astroparticle physics such as the study of solar and atmospheric neutrino interaction, the detection of neutrinos following a Supernova explosion, the study of neutrino oscillations with beams from particle accelerators, nucleon decay for some channels predicted by GUTs.

The apparatus consists of a very massive liquid Argon Time Projection Chamber (TPC), working as an electronic bubble chamber, continuously sensitive, with the ability to provide 3D imaging of any ionizing event.The first 600 ton module passed a technical validation run during 100 days in summer 2001 in Pavia, and is presently being installed under the INFN Gran Sasso Laboratory.

In this note we present the ICARUS trigger system, starting from the physics motivation to the details of the implementation including hardware and software aspects.

II. The ICARUS detector

The ICARUS T600 module is built inside a large cryostat split in two identical, adjacent half-modules, of internal dimensions $3.6 \times 3.9 \times 19.9$ m^3. The half-module houses a double Time Projection Chamber (TPC), with a shared central cathode and the readout wire planes placed on the lateral sides (fig.1), for a drift length of ~ 1.5 m. The chamber readout scheme consists of three parallel wire planes: the first facing the drift region, with horizontal wires (Induction I plane); the other two with wires at $\pm 60^\circ$ from the horizontal direction (Induction II and Collection planes, respectively). The total number of wires, and hence of independent readout channels, is more then 50000 for the T600 detector. The 3D image reconstruction of the event is provided by the signal of the electrons crossing the three subsequent wire planes, together with the measurement of the drift time (performed using a photomultiplier system). A detailed description of the ICARUS T600 detector is given elsewhere [1].

The ICARUS detector readout system is designed to provide continuous digitization and waveform recording of the signals from each wire of the TPC. The chain is composed of three basic units serving 32 channels:

- *decoupling* board (CAEN A764) receives analogue signals from the TPC wires and passes them to the analogue boards;
- the *analogue* board (CAEN V791) hosts the front-end amplifiers, performs 16:1 channel multiplexing and 10-bit digitization at 40 MHz rate (i.e. 400 ns sampling period on each channel, corresponding to 0.2 mm drift interval). It also provides the analog sum of the signals coming from 32 wires (AWS);
- the *digital* board (CAEN V789) provides the memory buffers, data reduction, processing and trigger logic. A memory pool can be segmented in programmable length circular buffers, from 64 to 4096 samples. In parallel the data stream is processed by the Daedalus chip [2], which detects the Region Of Interest of the incoming waveforms to provide data reduction capabilities [3]. Digitized data are accessible from the VME bus.

The readout scheme of the whole detector is organized in units each housing one VME-like analogue crate (with 18 analogue modules on the front and 18 decoupling boards on the backplane), one digital crate and the relative power supplies. Each rack handles 576 channels and includes a Motorola VME CPU as readout controller, the linear power supplies and the absolute time clock/trigger distribution.

III. The ICARUS Trigger system

Some of the most interesting, but extremely rare, events are those induced by a Supernova explosion. This phenomenon may produce a number of the order of 100 neutrino interactions in a few seconds in a 600 ton detector module. Such an event rate could not be handled if one aims at storing for each event the whole detector image (corresponding to 53248 wires). However, Monte Carlo simulations have shown that low energy neutrino interactions (such as those from a Supernova explosion) have a little occupancy of the detector, given the typical neutrino energy of a few tens of MeV.

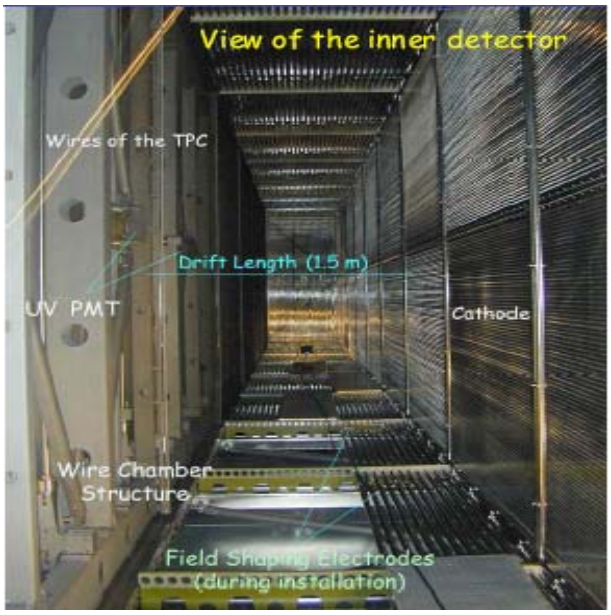

Figure 1: Photograph of the inside of one half-module during construction.

A few examples of events simulated in the ICARUS T600 detector are shown in fig.2. The proposed trigger system has the capability to select the volume around the event and only readout the few corresponding channels (local event), leaving the other unaffected channels free to record further events, thus reducing the global dead time.

A. The trigger architecture

The trigger scheme is based on three levels:

- the *L*ocal *T*rigger *C*ontrol *Unit* (LTCU) which reads the data from the TPC wires and from the PMTs and provides the first trigger level proposals. Each analogue crate can host one LTCU board;
- the *T*rigger *C*ontrol *Unit* (TCU) which implements the actual trigger logic. It performs a topological analysis of each event distinguishing between *local* and *global* events. The TCU provides the second trigger level proposals. According to the type, number and pattern of channels fired, an event is triggered as follows:
  - *global*, in this case the full detector is to be readout;
  - *local*, in this case the detector is partially readout.

  The whole detector can be handled by four TCU modules;
- the *T*rigger *S*upervisor (TS) which provides the trigger signal distribution, control, analysis and statistical monitoring of the system.

The schematic diagram of the trigger formation algorithm is shown in fig.3. The signals from the PMT and wires are discriminated by the first level trigger logic. If a majority condition is met in the PMT logic the event is classified as global. In this case the Trigger Supervisor has to distribute the trigger signal to all crates. On the contrary, if the majority conditions in the PMT logic are not met, an analysis of the signal from the wires is performed. A request coming from a limited number of crates is classified as local and the Trigger Supervisor has to distribute the trigger signal only to the interested crates. More details on the trigger classification will be given in the par.III-D.

The detector is said to be in a *global drift state* when a global trigger request from the TCU occurs. During this state the TS doesn't accept any other trigger request (local or global). It is said to be in a *local drift state* when the trigger request is local. In this case it doesn't accept any other local trigger request from the fired crates. At the end of the global drift time the detector switches to the *global busy state*. It will produce a DAQ dead time for the acquisition data download from all the chambers. During a global busy, the TS only accepts a local trigger request. In all cases, the TCUs will run the algorithms to determine the nature of the event, which can be labeled and counted accordingly. The entire system is built with programmable logic units based on state-of-the-art Field Programmable Gate Arrays (FPGAs).

B. The first trigger level-The Local Trigger Control Unit

The first trigger level [4] is implemented in custom hardware. The prototype is controlled through $RS232$ interface. The new version is controlled through a custom bus. Each LTCU receives as input 9 analogue sums from the Collection plane and 9 analogue sums from the Induction II plane. These signals are discriminated and logically OR-ed to produce the first level trigger proposals (T_0 and T_1).

The board is subdivided into two main stages: an *analogue stage* and a *digital stage* (fig.4). The former provides an high pass filtering and the input signal discrimination.

The latter is based on the FPGA device (Xilinx Spartan-2 [5]). It receives serial data (control word) from the external port, decodes it and executes one of the following operations:

- mask the noisy channels;
- set the comparators'threshold;
- give a test pulse to comparators' input;
- set the time window for rate measurements;
- read the rates for each input channel;
- put the comparator output on the front panel connector.

C. Test performance of the LTCU with a prototype detector

A prototype LTCU board (fig.5) has been tested on a liquid Argon TPC detector at CERN, exposed to cosmic-ray events. More details on the detector are available elsewhere [6]. The TPC is mounted inside a stainless steel cylindrical vessel, 65 cm in diameter, 90 cm in height, whose top face is closed by UHV flange housing the feed-throughs for vacuum, for liquid Argon liquid and high voltage and readout electronics. It has the shape of a parallelepiped whose details are shown in fig.6. A standard set of the ICARUS DAQ system has been used to acquire the events and to readout the 256 wires of the TPC. Both planes were readout with the current-like analog board V791C, via standard flat cables (whose length is the same as that of T600). The readout buffer size was chosen to be 1024 samples. We measured the LTCU efficiency using the setup shown in fig.6. A PMT, working in high efficiency conditions, has been used to provide the external trigger. The

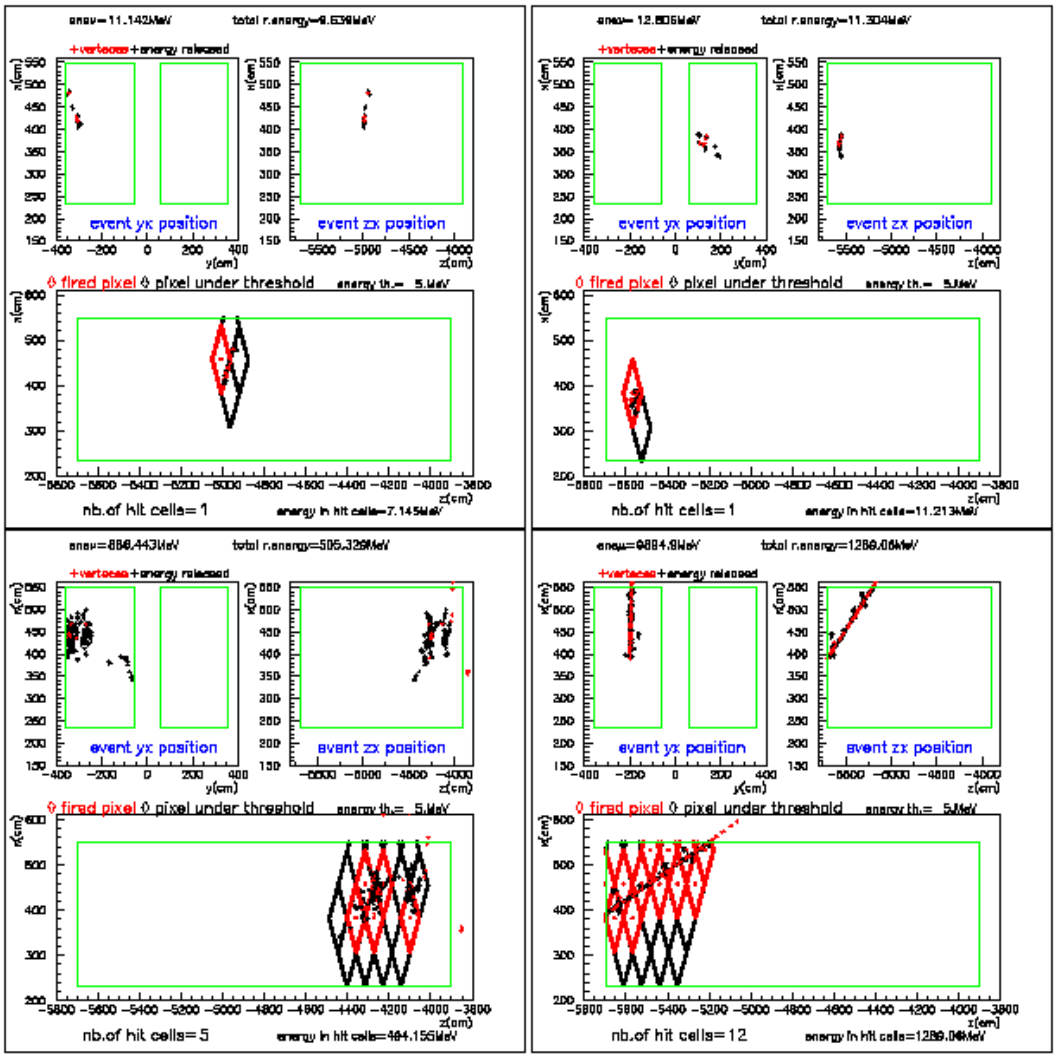

Figure 2: Simulated neutrino interactions ($\sim$ 11 and 900 MeV respectively) and passing muon ($\sim$ 10 GeV). Energy releases in the detector as seen in the two projections (top) and as reconstructed by the trigger (bottom). The fired zone is displayed in red.

trigger proposals from the LTCU have been recorded by the DAQ system. The efficiency is evaluated as the fraction of trigger proposals generated by the LTCU with respect to the total number of detected events as a function of the track incidence angle. The maximum measured efficiency is around 80%. This result can be ascribed to the noise of the board, estimated around 20 mV and due to the absence of a ground plane. The new board version, which will be soon available, is based on a new eight layers layout and additional shielding against environmental noise.

D. The second trigger level-The Trigger Control Unit

The TCU reads the trigger proposals from the first trigger level, performs the coincidences amongst the fired wires from the different planes and with the PMTs and validates the trigger proposals passing their addresses to the next trigger level. The elementary unit which contributes to define the picture of the event inside the detector is called *pixel*. It is defined by the coincidences between 32×9 wires from Collection plane and 32×9 wires from Induction plane (fig.7). The covered area is ~ 0.6 m^2. The TCU provides analysis of each incoming event distinguishing between *local* and *global* ones. In addition it determines a preclassification of the events on the basis of a comparison with MC predictions. In particular, the trigger classification depends on

- the energy deposition/number of fired PMTs;
- the detector occupancy;
- the 2D/3D pattern of fired pixels.

The signal from the Induction II plane is stretched up to $3\mu s$. This timing guarantees that the signals belonging to the different planes but corresponding to the same event can be seen in coincidence. The internal logic is divided into two main stages: a *front end* and a *trigger logic*. The *front end logic* has as inputs the trigger proposals from the first trigger level and produces a matrix containing the status of the fired pixels. It provides the synchronization of the data, the comparison of the signals width with remotely set thresholds, and makes coincidences amongst the fired wires. The *trigger logic* samples the pixels status every $100\mu s$, correlates the pixel status in subsequent images providing a rough image

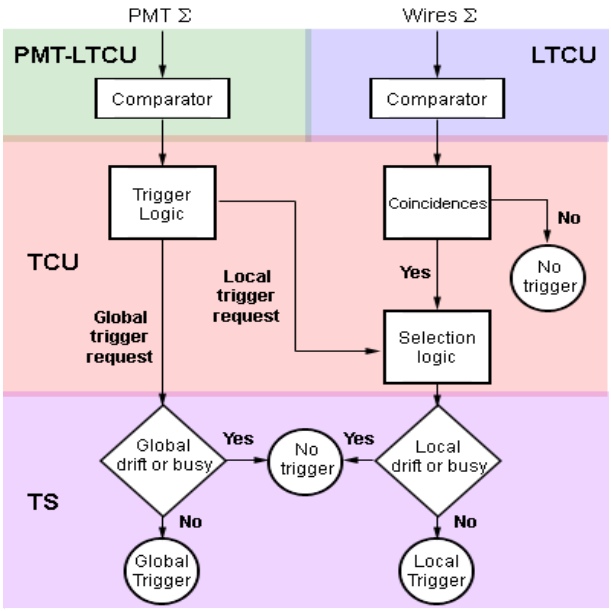

Figure 3: Trigger algorithm block diagram.

reconstruction and a preliminary event selection on the basis of the 2D/3D pattern of fired pixels and detector occupancy. It distinguishes between local and global events and produces the addresses of the fired pixels.

The second trigger level is preliminarily implemented on the UNIBOARD (fig.8) which is a general purpose board developed by the Detector and Electronic Service of INFN Napoli. It is a VME double height slave board with A32 D16, D32 data transfer capabilities. This board adopts a regular and flexible resources allocation scheme. The data coming from the the first level are transferred to the module via four 40 pin connectors hosted on the front panel.

The board consists of four identical stages each handling 20 differential inputs. The LVDS line receivers output is sent to four Front End FPGAs (XC2S100 -5PQ208 by Xilinx [5]) each serving a different slice of the wire planes. The elaborated data are redirected towards a synchronous dual port FIFO bank (IDT72V263). The FAUX manages the data stored in the FIFO bank and redirects them toward a mezzanine to be read by third trigger level.

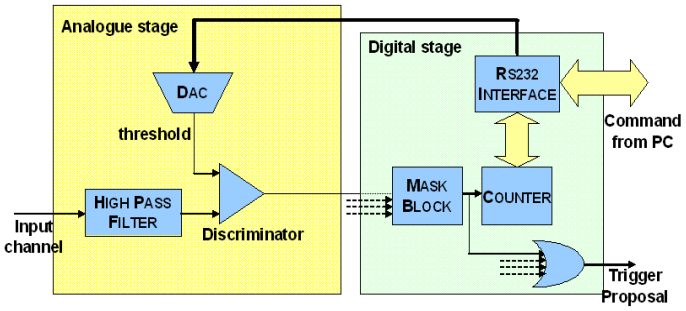

Figure 4: Local Trigger Control Unit block diagram.

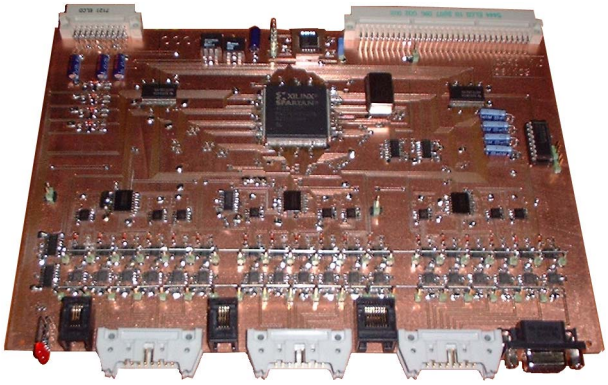

Figure 5: Local Trigger Control Unit prototype.

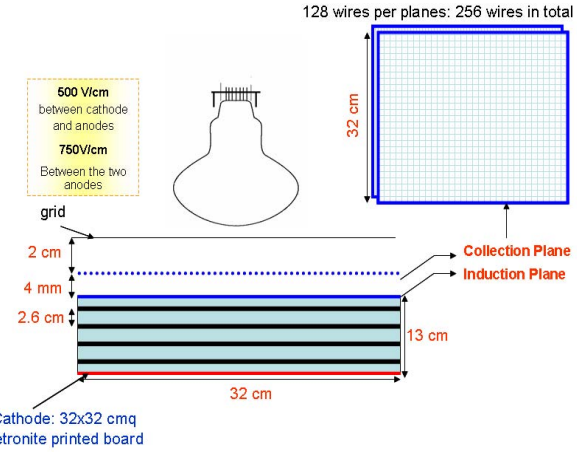

Figure 6: Setup for the LTCU efficiency measurement with details of the prototype TPC

E. The third trigger level-The Trigger Supervisor

The Trigger Supervisor is a VME module, receiving inputs from each chamber and the Absolute Clock. It validates trigger requests, performs trigger distribution and monitoring. Its basic design consists of 4 main blocks:

- the Trigger Generator block validates the trigger requests coming from the TCUs according to the DAQ status and distributes the trigger to the front end electronic;
- the Drift/Busy logic block which provides the interface with the DAQ system ;
- the Trigger TAG Builder block which tags the trigger events, assigning a trigger number, the absolute time and a label according to the event type;
- The State logic block which performs statistical computations such as the number of valid triggers, the number of global triggers, the number of local triggers etc.

IV. Conclusions

The trigger system of the ICARUS experiment is based on three levels and a segmented architecture. Its main aim is to be able to detect rare events, such as those coming from the explosion of a Supernova. The Local Trigger Control Unit, that processes the signals from the readout wire planes of the

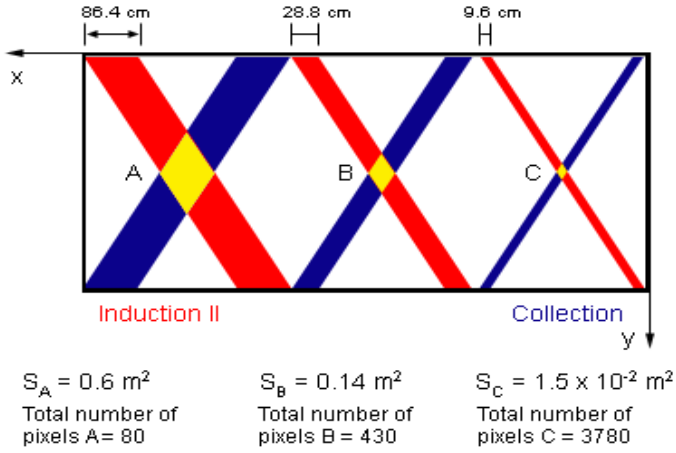

Figure 7: The wire plane section of a chamber is divided by the trigger system into pixels of different dimensions according to the segmentation chosen. A: 9 boards, B: 3 boards, C: 1 board.

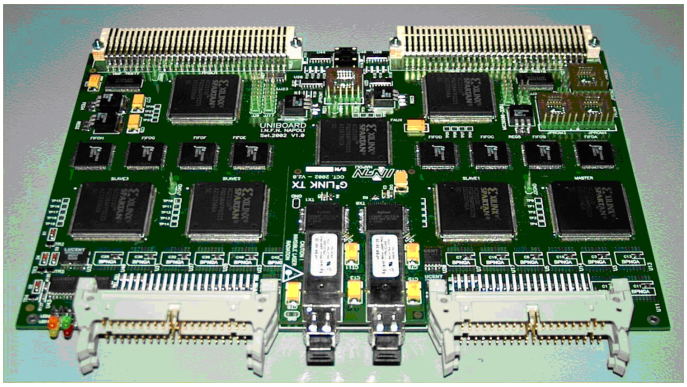

Figure 8: A possible implementation of The TCU: Uniboard module

detector, has been prototyped and tested on a TPC detector, in order to evaluate the noise conditions and fake trigger rate due to electronic noise. A new version of the LTCU is presently being mounted. The architecture and the design of the two higher trigger levels are presently being defined.

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REFERENCES

[1] ICARUS Collaboration, *Design, construction and tests of the ICARUS T600 detector*, Nucl. Inst. Meth., A527 (2004) 329-410.
[2] C.Carpanese et al., *Daedalus: a hardware signal analyser for ICARUS*,Nucl. Inst. Meth., A409(1998) 294-296.
[3] C.Carpanese et al., *Performance evaluation of a hit finding algorithm for the ICARUS detector*, Nucl. Inst. Meth., A412 (1998) 440-453.
[4] A.G.Cocco et al, ICARUS TRIGGER, *ICARUS-TM/04-13*, Internal note (2004), ICARUS Internal note, available on request.
[5] Xilinx, *Spartan -2 FPGA Family*, Datasheets;
[6] F.Arneodo et al, *The ICARUS 50 l LAr TPC in the CERN ν Beam*, arXiv:hep:ex/9812006v1, 3 Dicembre 1998;