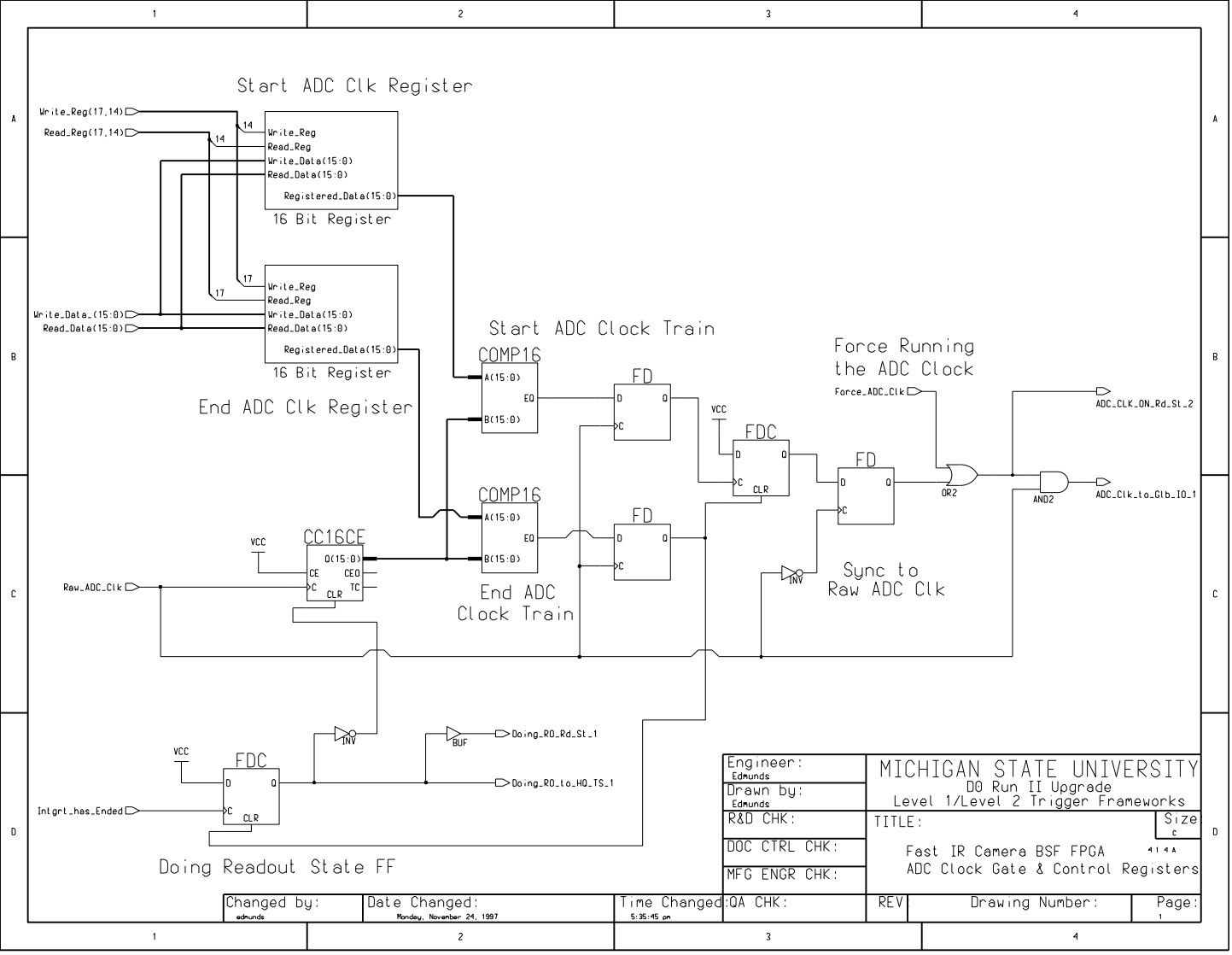

Changed by: edmunds	Date Changed: Monday, November 24, 1997	Time Changed: 5:35:45 pm	QA CHK:	REV	Drawing Number: / Page: 1

Engineer: Edmunds
Drawn by: Edmunds
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:

MICHIGAN STATE UNIVERSITY
D0 Run II Upgrade
Level 1/Level 2 Trigger Frameworks

TITLE: Fast IR Camera BSF FPGA
ADC Clock Gate & Control Registers

Size: C