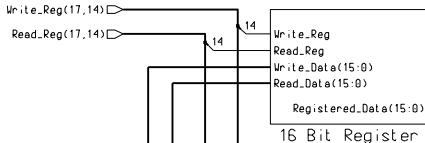
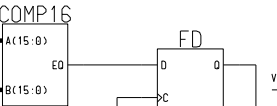


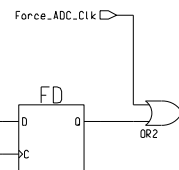
### Start ADC Clk Register



### Start ADC Clock Train



### Force Running the ADC Clock



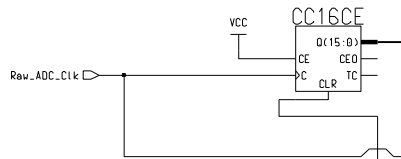
### End ADC Clk Register



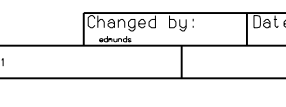
### End ADC Clock Train



### Sync to Raw ADC Clk



### Doing Readout State FF



Engineer: Edmunds	MICHIGAN STATE UNIVERSITY	
Drawn by: Edmunds	DO Run II Upgrade Level 1/Level 2 Trigger Frameworks	
R&D CHK:	TITLE:	Size c
DOC CTRL CHK:	Fast IR Camera BSF FPGA 4144	
MFG ENGR CHK:	ADC Clock Gate & Control Registers	
Changed by: edmunds	Date Changed: Monday, November 24, 1997	Time Changed: 9:35:45 am
QA CHK:	REV	Drawing Number:
		Page: 1