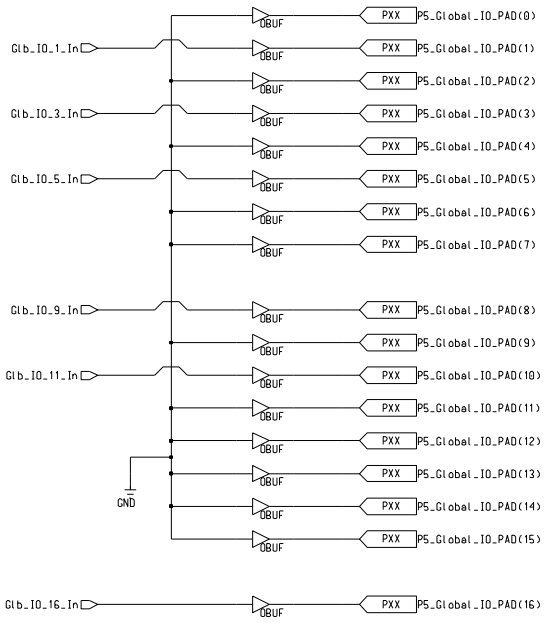

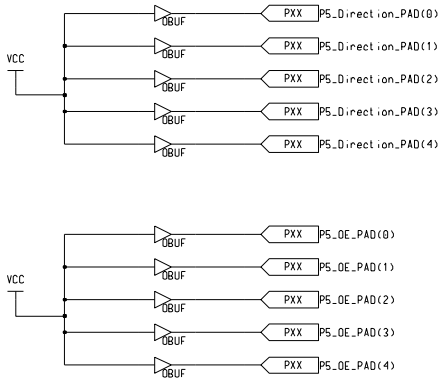

Direction Control

Hi --> TTL Input ECL Output

Low --> ECL Input TTL Output

Output Control

Hi --> Enable

Low --> Disable

Changed by: Edmunds	Date Changed: Saturday, November 22, 1997	Time Changed: 8:14:28 am	QA CHK:	REV	Drawing Number:	Page: 1

Engineer: Edmunds

Drawn by: Edmunds

R&D CHK:

DOC CTRL CHK:

MFG ENGR CHK:

MICHIGAN STATE UNIVERSITY

D0 Run II Upgrade

Level 1/Level 2 Trigger Frameworks

TITLE:

P5 Global IO Output Buffer

Fast IR Camera BSF FPGA

Size: C

4 1 4 A