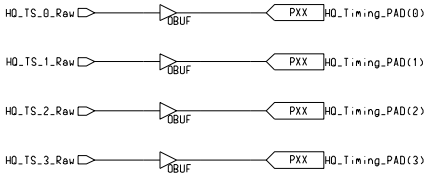

Changed by: Edmunds	Date Changed: Wednesday, November 19, 1997	Time Changed: 6:13:14 pm	QA CHK:	REV	Drawing Number: 4 1 4 A

Engineer: Edmunds
Drawn by: Edmunds
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:

MICHIGAN STATE UNIVERSITY
D0 Run II Upgrade
Level 1/Level 2 Trigger Frameworks

TITLE:
HQ Timing Signal Output Buffer
Fast IR Camera BSF FPGA

Size: C

Page: 1