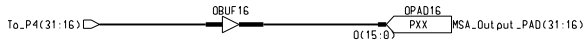

Changed by: Edmunds	Date Changed: Saturday, November 29, 1997	Time Changed: 3:43:33 pm	QA CHK:	REV	Drawing Number: / Page: 1

Engineer: Edmunds
Drawn by: Edmunds
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:

MICHIGAN STATE UNIVERSITY
D0 Run II Upgrade
Level 1/Level 2 Trigger Frameworks

TITLE:
P4 16 Bit Output Buffer
FIRC MSA #4 FPGA

Size: C
4 1 4 A