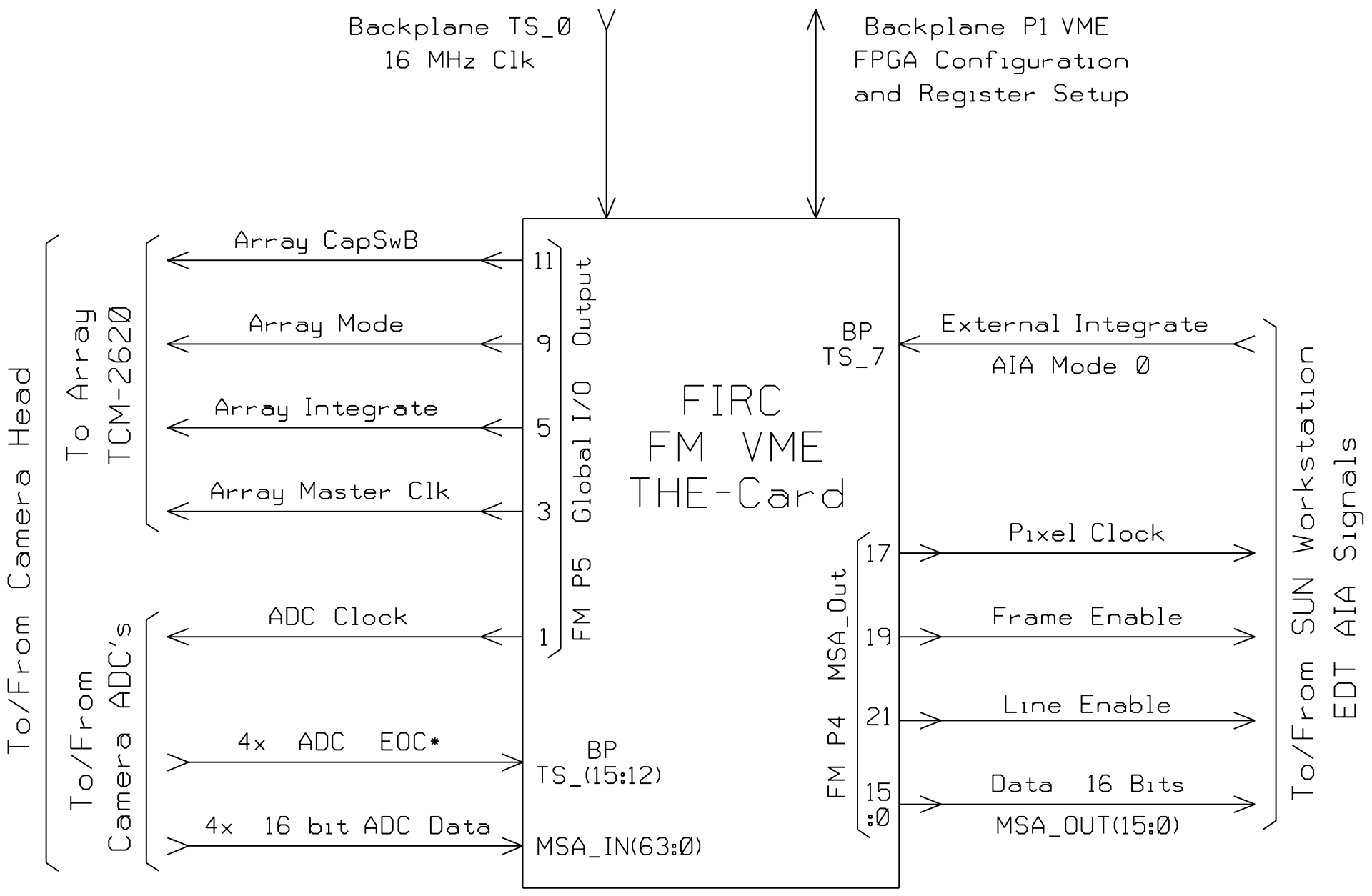
Backplane TS_0
16 MHz Clk
Backplane P1 VME
FPGA Configuration
and Register Setup
FIRC
FM VME
THE-Card
To/From Camera Head
To Array
TCM-2620
Array CapSwB
Array Mode
Array Integrate
Array Master Clk
11
9
5
3
FM P5 Global I/O Output
To/From
Camera ADC's
ADC Clock
1
4x ADC EOC*
BP
TS_(15:12)
4x 16 bit ADC Data
MSA_IN(63:0)
BP
TS_7
External Integrate
AIA Mode 0
FM P4 MSA_Out
17
19
21
15
:0
Pixel Clock
Frame Enable
Line Enable
Data 16 Bits
MSA_OUT(15:0)
To/From SUN Workstation
EDT AIA Signals