

Hybrid CMOS Focal Plane Array with Extended UV and NIR Response for Space Applications

Y. Bai*, S. G. Bernd, J. R. Hosack, M. C. Farris, J. T. Montroy, J. Bajaj
Rockwell Scientific Company, 5212 Verdugo Way, Camarillo, CA 93012

ABSTRACT

Silicon-based hybrid CMOS focal plane array technology offers many advantages needed for both ground-based and space imaging applications. These advantages include enhanced UV and NIR sensitivity, extensive on-chip readout capability, inherent radiation hardness, flexible imaging readout and the ability to provide extremely low noise at high video rates. For infrared imaging applications that involve UV-through visible channels, the readout electronics commonality facilitates a great simplification to system designs. In this paper, Rockwell Scientific CMOS-based hybrid silicon FPA technology and the recent progress are presented. The hybrid FPAs developed include 640x480, 1024x1024 and 2048x2048 formats with pixel sizes ranging from 27 μ m to 18 μ m square, featuring a high optical fill factor (~100%), broad-band response (200nm to 1000nm) with high quantum efficiency, and low read noise (<6e-) that approaches astronomy CCDs at 100KHz video rate and surpasses astronomy CCDs at 1MHz rate. Other performance parameters, such as spatial uniformity, dark current, pixel crosstalk/MTF and CMOS features are also discussed.

Keywords: CMOS, Hybrid, FPA, UV-Vis-NIR, Silicon detector array

1. SENSOR TECHNOLOGY FOR SPACE APPLICATION

1.1. CCD and CMOS

The key requirements for a sensor assembly to operate in space environments are high reliability, low weight, low power and high tolerance to radiation damage. Since its invention in 1969¹, silicon charge-coupled device (CCD) has improved in performance and built its flight heritage. Both size and format of CCDs have increased in the past several years for much-improved field-of-view and imaging resolution. This technology has been made available for various space missions, such as Galileo spacecraft² and Hubble Space Telescope³. However, concerns about CCDs in space exist due to charge transfer degradation in radiation environments, excessive power consumption, blooming and image smearing.

CMOS-based monolithic image sensor is another class of solid-state electronic imaging sensor that is rapidly evolving along with the advances in modern sub-micron CMOS technology. CMOS sensors offer important solutions to the CCD limitations encountered for use in orbit. The operation of CMOS sensors requires only one charge transfer (pixel-based charge-to-voltage conversion) for signal readout, consumes a very low power (typically operated at 3.3V and lower), and enables miniature cameras with on-chip integration of analog and digital circuitry, which significantly reduces the system mass, volume and complexity. In addition, the CMOS sensor can operate in a wide temperature range (cryogenic to 350K). CMOS wafer fabrication can use the mainstream commercial semiconductor foundries, and the cost of fabricating a monolithic 200mm CMOS wafer is less than that of a 150mm wafer using a specialized CCD process. More importantly, the CMOS imager is inherently tolerant to radiation damage. Space missions employing CMOS sensors, such as Deep Space-1 (256x256 format APS)⁴ and TEAMSAT (512x512 format APS)⁵, have provided encouraging science data and high contrast images.

Adding ultraviolet sensitivity to broadband visible imaging sensors increases the density of information for improved detection of targets. For scientific applications, the backside-illuminated CCD image sensor has been the technology of choice for enhanced quantum efficiency (QE), ultra-low noise, and large format. However, due to its thin device structure (~15 μ m), CCD QE response falls rapidly in the near infrared (NIR) band (>750nm), and non-optimized device

* Correspondence Email: ybai@rwsc.com; Web: <http://www.rockwellscientific.com/imaging/index.html>

optics typically results in interference fringes in the long wavelength QE response⁶ due to the multiple bounces of long wavelength light. The lack of sufficient NIR sensitivity can be a limitation for some crucial imaging applications, such as cosmological observations involving red shift⁷ and multi-band spectroscopic instruments that require a significant overlap between spectral channels. From the optical sensitivity standpoint, the monolithic CMOS sensor also has some performance limitations, such as lower optical fill factor (<60%) due to in-pixel amplification circuitry, lower peak quantum efficiency (~60%) in the photo-diode, and relatively low spectral response in blue and NIR wavelength regions. The lack of UV response imposes a crucial limitation on monolithic CMOS sensors for applications like astronomical detection of young, hot stars, atmospheric remote sensing and earth observing. These limitations have led to the development of a CMOS-based hybrid sensor⁸ that uses a silicon detector array to optimally perform photon-to-charge conversion while retaining excellent CMOS functionality. In this case, the CMOS chip is used as a readout element.

1.2. Hybrid CMOS Focal Plane Array Architecture

A hybrid FPA is composed of two components: detector array and readout multiplexer. The detector array is responsible for photon-to-charge conversion and the readout multiplexer functions as a charge-to-voltage converter and signal processor. Two components are precisely aligned and hybridized together through indium interconnects. Figure 1 illustrates the structure of hybrid CMOS silicon FPA. The unique feature of this hybrid is that both components are *optimized independently* to maximize the detection sensitivity and chip functionality. This hybrid approach can cost more than the monolithic counterparts due to the extra fabrication steps required, but the unique design and structure make it potentially an ideal candidate for achieving the ultimate scientific detector performance.

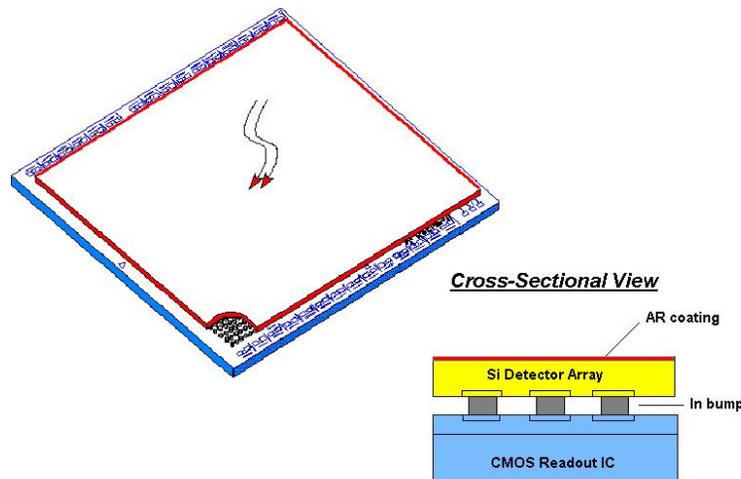


Figure 1. Schematic of hybrid CMOS visible Focal Plane Array

The material and structure for photovoltaic detector can be tailored for the desired spectral band coverage and operating temperature. Detector material choices include wide band-gap materials (GaN, GaAs) for UV-Visible detection, mid band-gap silicon material that responds favorably to UV-visible-NIR photons, and the commonly used narrow-band infrared materials (HgCdTe, InSb and InGaAs). A silicon-based detector allows the full exploration of a high quantum efficiency and simultaneous broad spectral coverage from UV, visible to NIR. In addition, this vertically-integrated structure allows the realization of 100% optical fill factor, and the readout design to utilize the whole pixel site either for added functional circuitry or enhanced charge handling capacity. This design becomes even more advantageous when more gain stages, snapshot imaging, and on-chip correlated double sampling (CDS) are needed. The “memory-like” pixel addressing with rows and columns enables functions like electronic shuttering, windowing (direct readout of region-of-interest at high frame rate) and the ease of pixel binning (summing or averaging for better S/N). Because it can be implemented using commercially available radiation-hard CMOS process and radiation hard designs, this sensor can be made inherently tolerant to radiation damage. From a system integrator standpoint, two other features are particularly attractive. This hybrid structure can possess all attributes of modern CMOS imager, including System-on-Chip (SoC). When multi-channel sensor system is deployed, the commonality of readout multiplexer and drive-electronics with infrared channels is another unique attribute that brings significant cost and risk savings at the system level.

In the following sections, the technology merits of this CMOS-based hybrid visible FPA developed at Rockwell Scientific will be analyzed in conjunction with detector performance, interface electronics, radiation hardness and its implications to diverse high-end applications.

2. HYBRID CMOS SILICON TECHNOLOGY AT ROCKWELL SCIENTIFIC

Silicon is a natural detector material choice for visible-band detection and imaging. When it is properly designed and fabricated, a silicon detector can offer a high spectral sensitivity from UV band to NIR band. The hybrid CMOS silicon FPA technology at Rockwell Scientific (RSC), called HyViSI™ (*Hybrid Visible Silicon Imager*), is constructed using a highly sensitive silicon photodiode array, advanced sub-micron CMOS readout multiplexer and precision flip-chip hybridization technology. The detector array design is based on the designs of high performance silicon photodiode and tailored to an array format and thin structure. Detector designs focus on high quantum efficiency, extended spectral band, low dark current, ultra-large format and radiation hardness. CMOS readout multiplexers developed at RSC feature low noise, large dynamic range, high speed, and various formats. The recent readout development emphasizes increasing on-chip functionality using deep sub-micron CMOS ($\leq 0.25\mu\text{m}$). Silicon detector arrays have been designed and fabricated in a number of formats and pixel sizes and can be hybridized to virtually any matching readout chips developed at RSC. Currently, we are producing high performance visible FPAs in 640x480, 1024x1024 and 2048x2048 formats. We have also fabricated 2048x2048 FPAs using the recent three-side buttable HAWAII-2RG⁹ readout chip with added features for use in either single chip or mosaic configuration. These FPAs have demonstrated many performance advantages, such as high quantum efficiencies, extended spectral response band and low dark current. These devices have been delivered to a number of customers involving ground, airborne and space applications. Table 1 summarizes the hybrid CMOS FPAs that are currently in production at RSC. Figure 2 show the actual FPA samples in various formats and camera systems.

Table 1. List of hybrid CMOS silicon FPAs currently in production at Rockwell Scientific

	PICNIC	TCM2620	TCM6604A	TCM8050A	HAWAII-1RG	HAWAII-2RG	
Input Circuit	SFD	CTIA	CTIA	DI	SFD	SFD	-
Array Format	256x256	256x256	640x480	1024x1024	1024x1024	2048x2048	Pixels
Pixel Pitch	40	40	27	18	18	18	μm
Number of Output	4	4	4	4	1, 2, or 16	1, 4 or 32	-
Nominal Pixel Rate	0.25	8	8	6	0.1 to 5	0.1 to 5	MHz
Read Out Mode	Ripple	Snapshot	Snapshot	Snapshot	Ripple	Ripple	-
Window Mode	na	na	Programmable	Full, 512, 256	Guide window	Guide window	-
Peak QE	90	90	90	90	90	90	%
Spectral Band	200-1050	200-1050	200-1050	200-1050	200-1050	200-1050	nm
Charge Capacity	200	2,000	700	3,000	100	100	Ke-
Read Noise	<20	<120	<100	<300	<10	<10	e-
Power Dissipation	<1	<60	<70	<100	<1	<4	mW



Figure 2. Development chronology for hybrid CMOS silicon focal plane arrays at Rockwell Scientific

3. PERFORMANCE CHARACTERISTICS

All imaging sensors can be evaluated using a similar set of performance parameters. In the following sections, we review the status of RSC silicon focal plane array performance.

3.1. Quantum Efficiency, Response Uniformity and Linearity

High quantum efficiency relies on the effective control of external optical reflection and internal electrical losses of a detector. The silicon detector array developed operates in a back-illuminated mode. When combined with a fully depleted device design, the spectral response can cover a broad wavelength band ranging from UV to NIR. At UV wavelengths ($\leq 400\text{nm}$) where the incident photons are absorbed very close to the silicon surface, the surface design and treatments are important. In the near infrared band ($> 750\text{nm}$), a sufficient silicon absorber is essential due to the indirect band gap of silicon. Beyond the wavelength of greater than 1100nm , silicon becomes transparent and QE cuts off rapidly. Depending on specific applications, optical coating also is important in boosting QE and emphasizing the spectral band of interest (i.e., UV, Vis, NIR or broad band). Figure 3 shows spectral QE data measured on PEC (process evaluation chip) devices with various antireflection coatings. Both PEC device and detector array were fabricated together on the same wafer. FPA data were taken using a set of narrow band-pass filters and agree well with PEC QE data. A high quantum efficiency (peaks at 90%) response has been measured, and the spectral response of detector covers the wavelengths ranging from 200nm to 1050nm . A detailed QE analysis indicates that the optical reflection loss is the dominating loss component and QE can be improved by an optimized antireflection coating design either with single layer or multiple layers.

The uniformity of silicon material and the effectiveness of device processing determine the pixel operability and spatial uniformity across a silicon detector array. The operability also depends on the indium bump inter-connectivity as the result of flip-chip hybridization, especially for the large format arrays. We have routinely measured a uniform photon-response ($\sigma/\text{mean} < 2.5\%$). High operability was also measured on large format arrays. For example, QE operability ($> 80\%$ QE mean) was measured at 99.99% for 640×480 array with $27\mu\text{m}$ pixel size. A 99.99% pixel operability has also been measured on 2048×2048 format array with $18\mu\text{m}$ pixel size. Figure 4 shows a QE histogram taken on a 2048×2048 format HAWAII-2RG HyViSI™ FPA under a “flat” field illumination. The inoperable pixel count (with $\text{QE} < 60\%$) is only 233 out of 4.16 million pixels. The second small peak in the histogram is due to a non-uniform illumination (the center of the array received more photons).

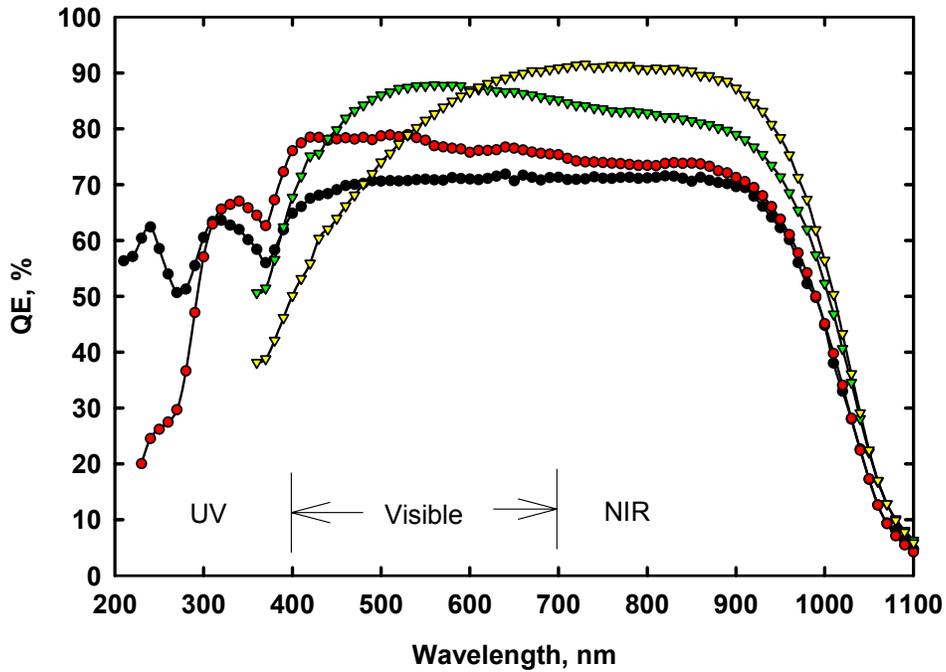


Figure 3. Measured spectral QEs for hybrid CMOS silicon focal plane arrays. Single layer antireflection coating is used for all curves and each curve has a different coating design (Temperature = 295K)

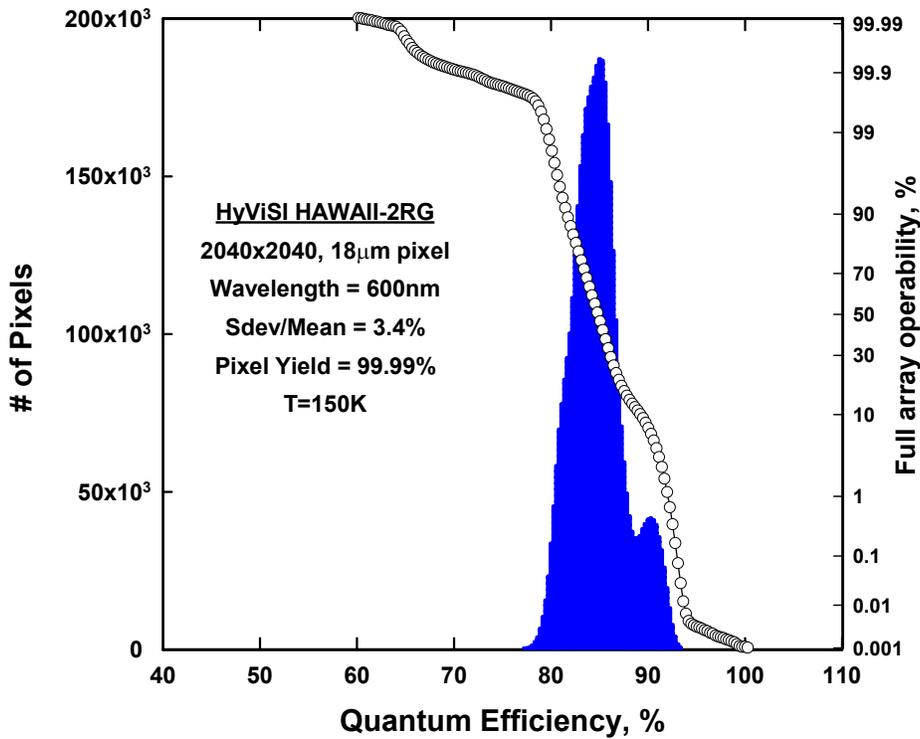


Figure 4. QE histogram and pixel operability (for pixels with QE \geq 60%) as measured on a 2048x2048 format HAWAII-2RG visible FPA (4 outer reference rows/columns are excluded)

NIR response and the temperature dependence of QE cut-off wavelength are of interest for applications that require cryogenic operation. Because of silicon band gap increase at lower temperatures, QE cut-off wavelength reduces accordingly. The temperature dependence of spectral QE was therefore evaluated for both FPA and PEC devices in a broad temperature range (room temperature to 78K). Figure 5 shows the spectral QEs in the NIR band measured at two temperatures. From room temperature to 78K, the measured cut-off shift is about 50nm. The shift predicted from the temperature dependence of silicon band gap is around 40nm for the same temperature range. The difference is due to the finite thickness of silicon detector. Also shown in Figure 5 is that the temperature dependence of long wavelength responses becomes insignificant for wavelength less than roughly 900nm.

Detector photo-response linearity depends on the type of input circuit design and the interface with silicon detector. Among three types of input circuits that are commonly implemented in our CMOS readouts, i.e., source follower per detector (SFD), capacitive trans-impedance amplifier (CTIA), and direct injection (DI), the response non-linearity for near full well was measured at <4% for SFD, <1% for CTIA and <1% for DI.

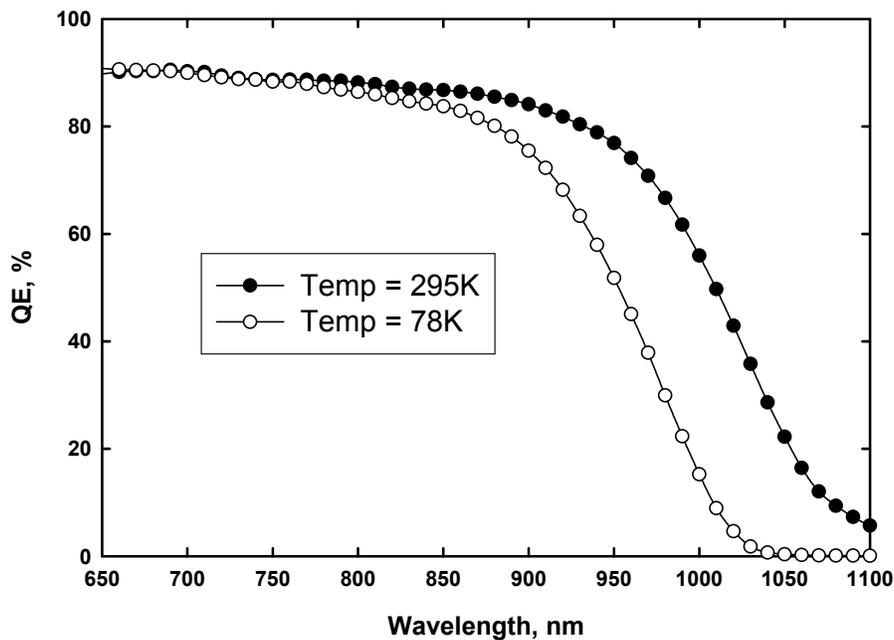


Figure 5. Measured temperature dependence of spectral quantum efficiency

3.2. Read Noise, Dark Current, and Dynamic Range

The temporal noise from silicon FPA is composed primarily of read noise and dark current shot noise. Read noise depends on input circuit as well as the readout speed (pixel rate). Dark currents are thermally-generated and can be reduced by lowering sensor operating temperature. Sensor dynamic range is typically defined as the ratio of charge handling capacity to noise floor.

The unique readout architecture of a CMOS imager and pixel-based amplification offer a fundamentally reduced noise bandwidth and a low resulting read noise¹⁰. In CCDs, both charge-to-voltage conversion and video signal buffering occur at output stage and the ultra-low read noise (a few e-) is made possible only by limiting video bandwidth to several tens of kHz. This can be an issue for the applications requiring a large format. When coupled with a low capacitance silicon photodiode, lower read noise and higher conversion gain are expected in the silicon-based hybrid CMOS imager. Among several types of pixel-based input circuits, SFD is a very low noise readout input circuitry widely used for applications involving a low background and long frame time. CTIA is a low noise, high speed input circuit; and DI circuit is more suitable to mid to high background, high-speed application.

Figure 6 shows the mean read noise measured from CMOS-based imaging sensors for representative low-noise input circuits¹¹. The plot shows that noise is a strong function of effective sense capacitance at the input node. Reducing sense capacitance leads to lower read noise and higher conversion gain. The rms read noise data measured from several hybrid silicon FPAs in this CMOS-based dataset include 6e- for SFD, 70e- for CTIA and 250 e- for DI, with corresponding conversion gains of 7 μ V/e, 6 μ V/e and 3 μ V/e, respectively. The 6e- noise was measured at 250 kHz pixel rate and with a correlated double sampling (CDS). This is a level very competitive with the noise typically achieved at this video rate by astronomy CCDs. With Fowler sampling, we expect to have the read noise approaching 1e-, a level superior to that achieved with CCDs at lower video rates.

Also shown in the figure is a data point measured with a monolithic CMOS sensor using the source follower input amplifier in tapered reset mode¹². Tapered reset obviates the need for correlated double sampling to remove reset noise and is made possible in CMOS-based imaging sensors by their system-on-chip functionality. The average noise of 2.5 e- for the 30Hz frame rate measurement with 5.5fF detector capacitance represents over 10X reduction in reset noise without correlated double sampling.

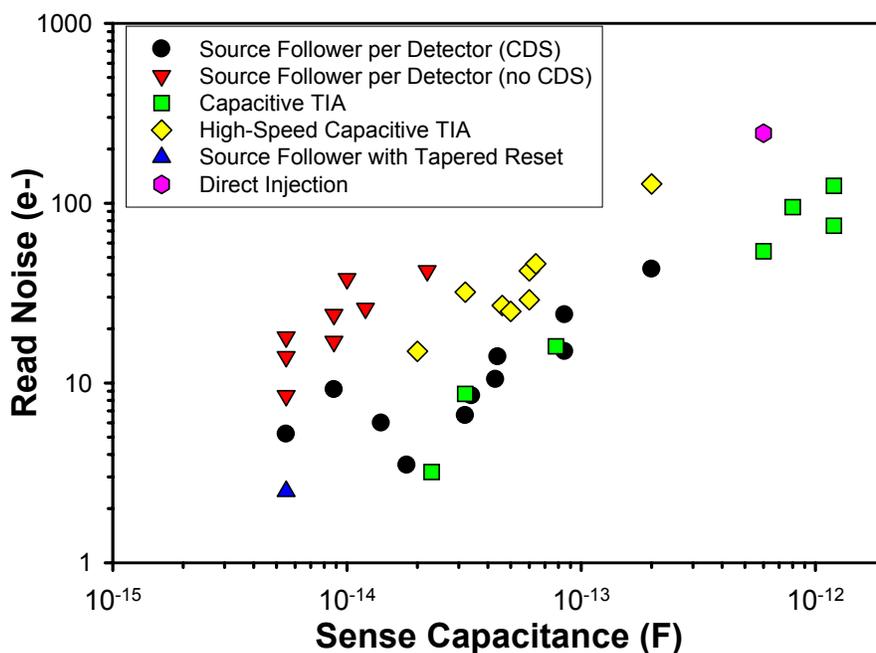


Figure 6. Read noise vs. sense capacitance for various imaging sensors at Rockwell Scientific.

Detector dark current is more technology-dependent. Multi-pinned-phase (MPP) scientific-grade CCDs still maintain the lowest dark current on the order of 50pA/cm² at room temperature. Monolithic CMOS imager is more dependent on the CMOS process used and the typical values around 300pA/cm² has been demonstrated. The principal sources for dark current are thermal electron generation in the depletion region and at the surfaces of detector, and can be reduced by cooling. The degree of cooling required depends on the longest integration time and the signal-to-noise ratio requirements. At room temperature, the dark current of the silicon detector array is limited primarily by bulk generation current, since the current follows a V^{1/2} bulk-dominated dependence. This component is determined by detector geometry, carrier concentration and carrier lifetime. Our current detector array dark current is measured at 5-20 nA/cm² at room temperature and another 10x reduction is expected. Part of the dark current source of the silicon detector is attributed to the relatively large device bulk that is used to boost NIR response (up to 1000nm). Other detectors, CCDs and monolithic CMOS, have a much thinner active detection layer. For low background applications, detector arrays need to operate at low temperatures, the same as CCDs. At these temperatures, detector dark current is typically no longer a bulk behavior. A combined optimization is required. We have measured ~1fA/cm² ultra low dark current in a temperature range of 100K to 150K. For example, 0.015 e-/sec/pixel dark current was measured at 100K using our

HAWAII readout with an 18 μm pixel pitch, and 0.1 e-/sec/pixel was measured at 140K using our PICNIC readout with a 40 μm pixel pitch.

The spatial non-uniformity of all pixels in the dark is related to the spatial non-uniformity of electrical characteristics of readout circuitry (in-pixel and other on-chip components) as well as the detector array. The static voltage spread of all pixels in the dark was measured at 0.5% ($\sigma/\Delta V$, uncorrected) for these large format arrays. Dark current non-uniformity was measured as low as 6% (σ/mean).

Referring to charge handling capacity, one unique feature of this hybrid structure is that it frees up more space in the pixel by moving the sensor element out of pixel site. The charge handling capacity of RSC existing readouts is up to 150Ke- for 18 μm SFD input, 700Ke for 27 μm pixel CTIA and 3.5Me- for 18 μm pixel DI input cell. The instantaneous dynamic ranges for these sensors are typically greater than 80dB.

3.3. MTF and Crosstalk

The imaging quality is evaluated by means of modulation transfer function (MTF). It represents the image sharpness or the spatial frequency response of an imaging sensor. The detector design is based on a backside illuminated and fully depleted operation mode. The photon generated charges transport vertically by drift mechanism under a strong voltage bias. In the lateral direction, there is no electrical field and the charge carriers move by diffusion mechanism, thereby causing image “diffusion”. The amount of charge diffusion is a function of bias and temperature. The wavelength is also a factor because the shorter wavelength light is absorbed closer to the illuminated surface and the resulting photon-generated charges must travel a longer path before being collected. The distribution of charge current at the collection junction follows a Gaussian function. Based on a near surface absorption assumption, the lateral charge spread can be characterized using a diffusion sigma defined as

$$\sigma_{diff} = d \cdot \sqrt{\frac{2kT}{qV}}$$

where d is the detector thickness and V is the detector bias. Diffusion sigma (σ_{diff}) decreases with a thinner detector and higher bias. In a frequency space, MTF is commonly used to characterize the image degradation caused by charge diffusion. MTF is the product of diffusion MTF and aperture MTF.

The calculated MTF curves are shown in Figure 7 for two different detector biases and at two temperatures. 18 μm pixel pitch is used for the calculation. Again, a near surface absorption is assumed. As shown in the figure, a high voltage bias, a low operating temperature or a combination of both is needed to achieve a MTF of 0.5 at Nyquist spatial frequency. Figure 8(a) is the USAF chart image taken with TCM6600A silicon FPA at 273K. Image resolution reaches pixel spatial frequency at ~8V detector bias. Figure 8(b) is a spot response map of the same type of device at 600nm wavelength and 15V bias. The grid spacing is 27 μm . For this single pixel illumination, the signal is well contained in the center pixel and only a very small portion of signal is collected at its *nearest* neighbors. If we define a pixel crosstalk based on this full-size pixel illumination case, the ratio of the signal collected by a neighbor pixel to the signal in the illuminated pixel is calculated to be less than 1%. Work is on-going to evaluate the full MTF characteristics.

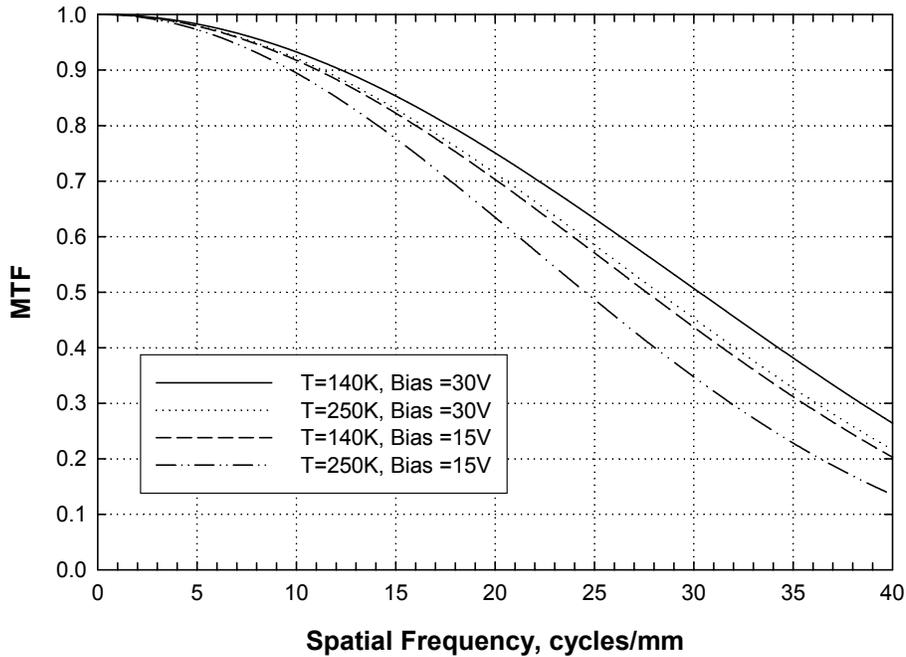


Figure 7. Calculated MTF as a function of detector bias and temperature for 18 μ m pixel detector array

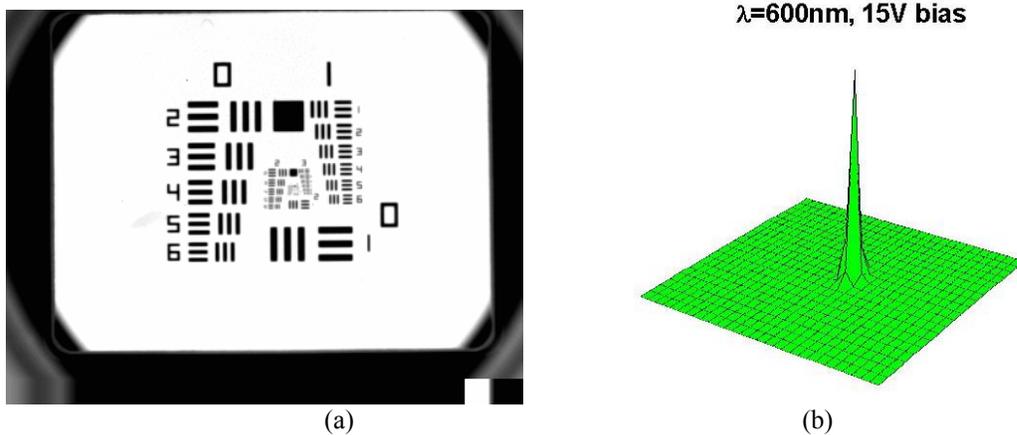


Figure 8 Captured image of USAF chart and Spot Response (SR) using a HyViSI TCM6600A FPA

3.4. On-Chip Features

Due to its CMOS nature, this hybrid FPA can benefit greatly from on-chip features of CMOS circuit designs. This hybrid structure is particularly suitable for implementing pixel-based snapshot capability without any compromise in optical fill-factor, charge capacity and chip size, as compared to interline CCDs and full frame CCDs. Both snapshot imaging mode (global shutter) and ripple mode (rolling shutter) are available for RSC CMOS readouts. TCM6604A and TCM8050A readouts are two examples with snapshot mode. Both chips have programmable windowing to custom sizes for either reading the region of interest (ROI) or boosting frame rate. In addition, CMOS is naturally immune to local bright or

overly exposed signals because the charge is contained within the pixel site and a charge draining mechanism can also be implemented in the pixel to avoid charge spilling to its neighboring pixels via detector.

On-chip integration of analog-to-digital conversion (ADC) is another feature that is being pursued actively at RSC¹³. 10MHz sampling and 10-12 bit ADCs are being standardized for several readout chips and higher resolution ADCs (14-16 bits) are being implemented for both hybrid and monolithic FPAs. A FPA control chip has also been developed. RSC SIDECAR¹⁴ is a single-chip, application-specific integrated circuit (ASIC) that combines all necessary functions to operate CMOS-based FPA and provide 12-16 bits digital data. It can be mounted side-by-side with FPA. This full-feature, low-power (<8.4mW), and system-on-chip controller is expected to allow system designers to have the true miniature camera system built in their scientific instruments.

3.5. Radiation Hardness

In space radiation environment, both ionizing and non-ionizing radiation can cause damage to silicon-based focal plane arrays. Total ionization dose (TID) effect, bulk displacement damage, and single-event effects are the common causes of sensor degradation. Because of the specific device structure of the hybrid devices and the different operating mechanisms in detector array and CMOS readout, radiation effects in detector and readout IC are different.

The silicon detector is a bulk-limited bipolar device, which provides some inherent protection to interfaces from ionization damage. Detector dark current is the main parameter relevant to radiation effects. The radiation-induced dark current increase is caused primarily by bulk displacement damage, which creates bulk structural defects that lead to degradation of carrier lifetime and mobility. To bring dark current in compliance after irradiation, a proper cooling with margin is typically implemented to meet the EOL dark current requirement. In contrast to bipolar devices, CMOS devices are more sensitive to ionization damage resulting from cumulative ionizing radiation exposure. This exposure usually leads to a charge buildup in silicon dioxide and an increase in interface trap density, leading to threshold voltage shift and FET leakage.

We have observed that the standard commercial sub-micron CMOS process (0.5 μ m) can frequently survive up to 35Krad (Si) of total ionization dose without parametric degradation. Beyond this dose up to 50Krad, the ROIC is still functional but parametric changes start to occur, mostly column degradation (different from CTE degradation). The degradation is attributed mostly to the MOS leakage current. Modifications to standard IC process are expected to increase the tolerance of CMOS circuitry up to 100Krad (Si). In fact, testing on recent RSC 0.25 μ m CMOS test devices showed TID hardness greater than 100Krad. For hardness beyond 100Krad up to a few Mrad (Si), special designs or dedicated rad-hard process are usually required. Currently, several types of RSC hybrid silicon FPAs are being systematically evaluated under both ionization and non-ionization environments. Preliminary data are promising.

4. SUMMARY

The advanced modern CMOS technology, high performance silicon detector arrays and reliable large-area flip-chip hybridization have made it feasible for hybrid CMOS silicon focal plane arrays to play a role in space missions. This technology offers a high performance alternative to existing CCDs in meeting high-end visible imaging needs when performance, radiation hardness, stability and ease of device operation are the main drivers. High performance FPAs in 640x480, 1024x1024 and 2048x2048 formats have been produced using a variety of CMOS readouts developed at Rockwell Scientific. The 2048x2048 format visible FPA has also been produced using our recent three-side buttable HAWAII-2RG readout chip for use in either single chip or mosaic configurations. The emphases of on-going efforts at RSC are ultra-low noise, high pixel density and larger format, high radiation tolerance, and the implementation of ASIC chip to further simplify FPA control at subsystem level. Based on the NASA technology readiness scale, our assessment of this technology is currently at TRL 6 & 7, i.e., flight validation stage.

5. ACKNOWLEDGMENTS

Authors acknowledge the technical support of our colleagues in the Imaging Division of Rockwell Scientific and the valuable discussions with many technologists who show great interest in this FPA technology. Inputs from Lester Kozlowski are greatly appreciated. UV QE data were obtained from the work at RSC under NASA Cross-Enterprise Program through Ball Aerospace & Technologies Corporation.

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