Hub - I2Cbus & multi-master

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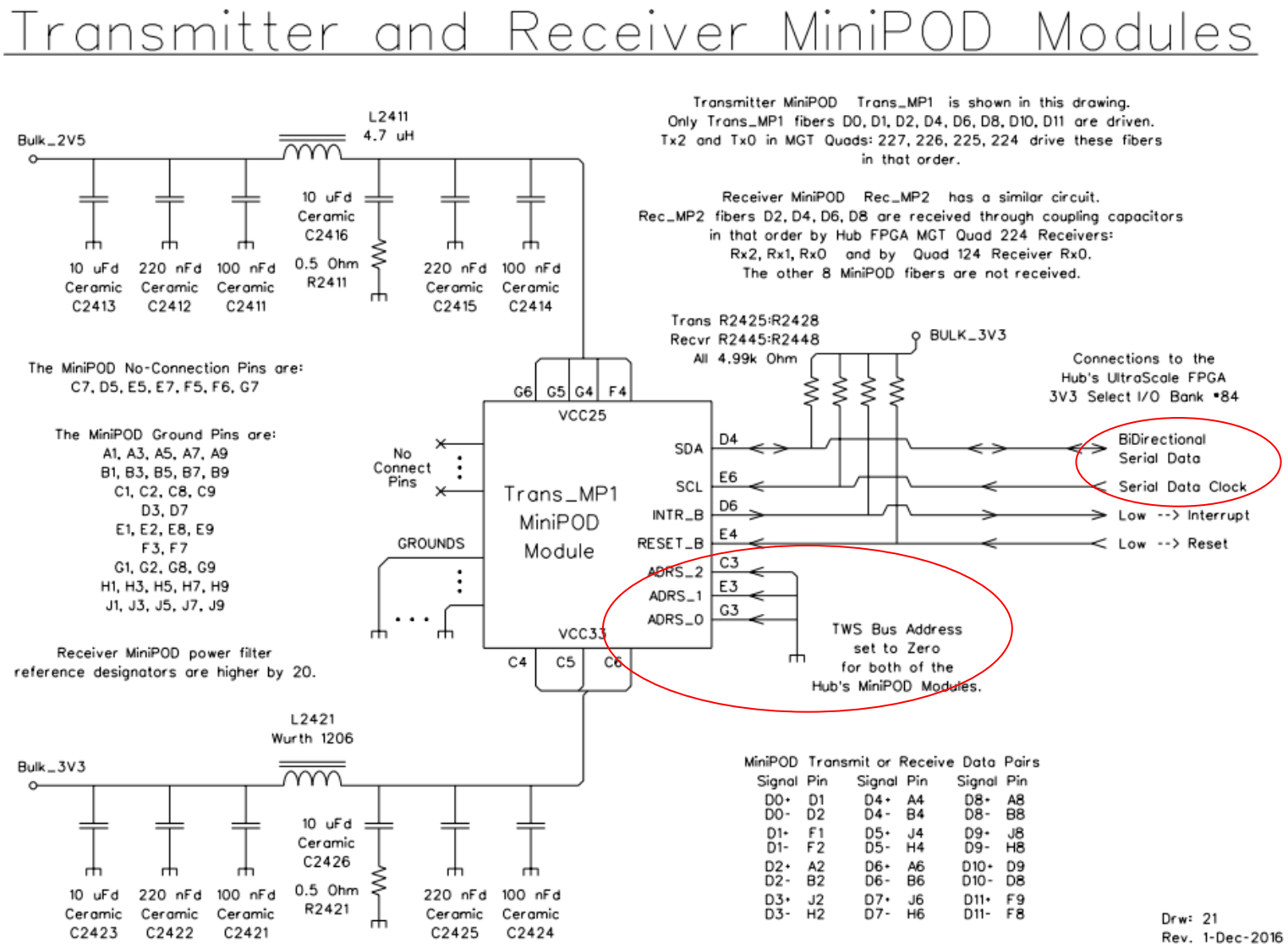
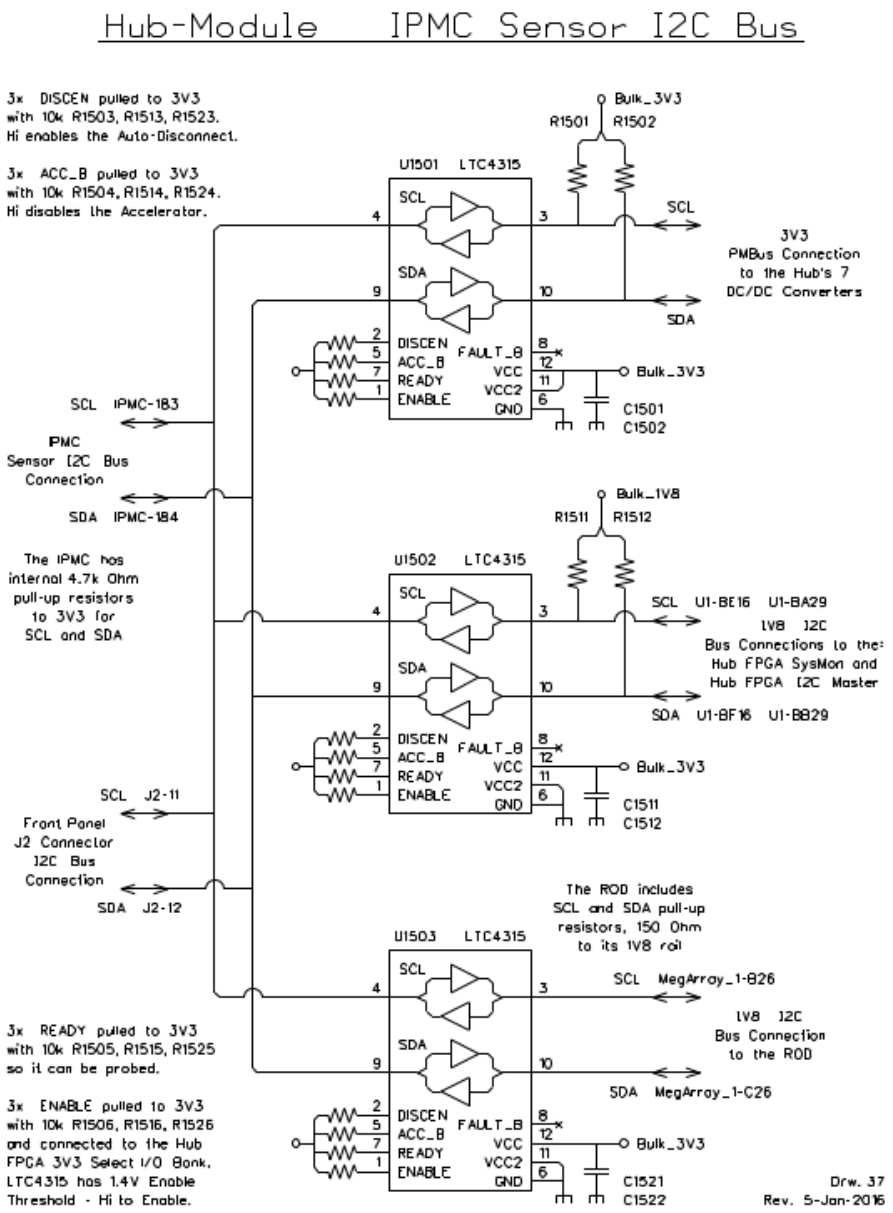
I2C @ MSU 4 L1Calo - a bit of history

- Started with legacy I2C state machine (RAL) for the CMM module
  - CoolRunner XPLA3 XCR3384XL 384 macrocell CPLD
  - Point-to-point access to TTCrx chip
  - Single master, no arbitration, simple (2 registers) interface
- Adapted for the CMX module
  - Spartan-3AN FPGA XC3S200AN-4FTG256C
  - Individual masters, no arbitration, point-to-point (TTCrx, MiniPOD, SFP)
- For the HUB, HW design started with the same idea
  - Initially Virtex7 FPGA, then move to Ultra Scale XCVU125
  - Single master, no arbitration, point-to-point:
    - ⇨ MiniPODs (Rx & Tx), DC/DC convertors (3 master I2C interfaces on FPGA)
  - Dedicated slave I2C interface to FPGA System Monitor
- For the HUB FPGA FW development use XILINX I2C IP
  - Full Master/Slave I2C, AXI4 interface, 22 control/status registers
  - IPbus to I2C via AXI4 bridge (Ed Flaherty, Cambridge)
- Then IPMC came into the game…

Rx & Tx MiniPODs I2C – access from IPbus



DC/DC, SysMon, ROD – IPMC Sensor I2C bus



- Access from IPbus:
  - To 7 DC/DC
- Access from IPMC:
  - DC/DC, SysMon, ROD
- Buffers controlled via Ipbus
- Test front panel I2C connector

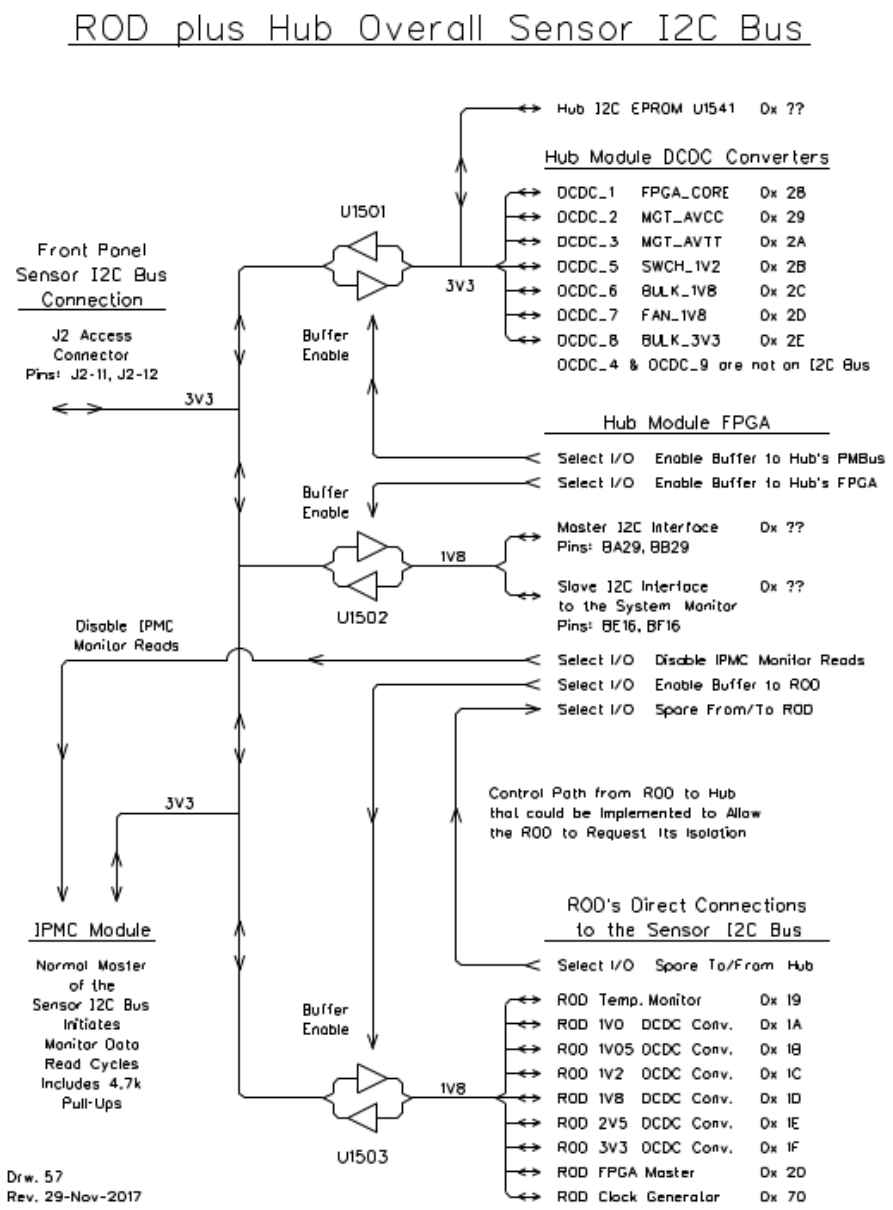
- Sensor I2C Bus

The IPMC Senor I2C Bus is used to collect monitoring data about power supply voltages and currents and device temperatures on the ROD and Hub. The IPMC will forward this hardware monitoring information over Ethernet to the Atlas DCS system. The layout of the Sensor I2C Bus is shown in drawings #37 and #57.

As shown in these drawings, three I2C bus buffer/translators are used both to drive the large number of devices on this bus, a combination of ROD and Hub devices, and also to translate between the sections of the Sensor I2C Bus that are 3V3 and the sections that are 1V8 signal level I2C bus. The buffer/translator part that is used on the Hub is the Linear Technology LTC4315. If necessary these buffer/translators can also be used to separate the various sections of overall Sensor I2C bus under control of the Hub FPGA.

At times other devices will need to initiate and master cycles on the Sensor I2C Bus, e.g. to setup parameters in the GE DCDC power converters on both the ROD and Hub modules. A User I/O input pin on the IPMC to disable its collection sweeps of monitoring data might be useful during the short and infrequent periods when other devices need to initiate and master cycles on this bus.

DC/DC, SysMon, ROD, IPMC – addresses



I2C Addresses on the Hub-ROD Sensor I2C Bus:

	7 Bit Binary	Decimal	TI-GE Octal	Hex
ROD				
FPGA Master	0100 000	32	--	20
LM82 Temp Monitor	0011 001	25	--	19
MDT040 1V0	0011 010	26	32	1A
MDT040 1V05	0011 011	27	33	1B
PDT012 1V2	0011 100	28	34	1C
PDT006 1V8	0011 101	29	35	1D
PDT006 2V5	0011 110	30	36	1E
PDT006 3V3	0011 111	31	37	1F
SI5338 Clk Gen	1110 000	112	--	70
Hub				
FPGA I2C Master	0110 110	54	--	36
FPGA SysMon Slv	0111 000	56	--	38
MDT040 FPGA_CORE	0101 000	40	50	28
UDT020 MGT_AVCC	0101 001	41	51	29
UDT020 MGT_AVTT	0101 010	42	52	2A
PDT012 SWCH_1V2	0101 011	43	53	2B
PDT012 BULK_1V8	0101 100	44	54	2C
UDT020 FAN_1V8	0101 101	45	55	2D
PDT020 BULK_3V3	0101 110	46	56	2E

Notes about this Address Table:

Recall that a number of I2C addresses are reserved:
0:12, 40, 44, 45, 55, 64:68, 72:75, 99, 120:127
all in decimal.

I2C addresses are only 7 bits long (not 8 bits).

The MSB of the I2C address of the GE/TI converters must be zero.

TI-GE Octal means take the 6 least significant address binary bits and represent them as 2 octal digits, i.e. the setup of the address programming resistors on the TPS40400.

Decimal means take the whole 7 bit I2C address and represent it as a decimal number.

HUB DCS I²C buses