GBT-FPGA Tutorial
27 June 2016 (11 :00-18 :30)
Provisional Programme

https://indico.cern.ch/event/532419/

11:00 – 12:30: GBT-FPGA Overview

Introduction:
- What is the GBT-FPGA (supported FPGAs, principle, targeted applications)?
- What are the different blocks implemented?

Importing and Integrating the Block into your project
- SVN repository Architecture
- How to use the latest version of the GBT-FPGA (tortoise SVN, checkout)
- How can I use the GBT-FPGA in my project (What folders/files are required? What can be removed? Which files must be sourced)?
- How to use the tcl script provided with the project?
- How to customize the device specific part (PLL type, Transceiver type, reconfiguration bus, monitoring tools)?

12:30 – 13:30: LUNCH

13:30 – 15:00: Creating a Reference Design in Standard Mode

Demo setup (Arria 10 based)
- What is the setup (development kit + FMC TTC-PON)?
- What is my clock scheme?

Creation of a reference design from scratch (reusing GBT-FPGA blocks)
- How to create the project (new project, file sourcing ...)
- How to implement the GBT-FPGA using records (standard mode)
- How to implement required additional modules for standard mode (pattern generator/checker, clocking resources)
- How to extend the design to multi-links for a single bank (standard mode)
- How to configure the design for debug (standard mode)
- How to test the design (standard mode)

15:00-15:20: Coffee BREAK

15:20 – 16:20: Creating a Reference Design in Latency Optimized Mode

- What are the critical points of the Latency-optimized mode
- How to improve the design to run in latency-optimized mode
- How to set the right constraints for the latency-optimized mode
- How to configure the design for debug (Latency-optimized mode)
- How to test the design (latency-optimized mode, phase calibration)
- How to use the generic module designed to make a multiple bank design?

16:20 – 17:00: Using an existing Reference Design: case of the KC705

Using the existing example design

- How to test the KC705 example design?
- Specificities of the KC705

17:00-18:00: Tips and Tricks

- What do I have to take care when I design my hardware (clock scheme)?
- Which external PLLs are recommended?
- What are the devices specificities?

Discussion and Questions