HUB: Combined_TTC/DATA status

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Combined_TTC/DATA overview

- HUB is obliged to distribute TTC information throughout the shelf. Combined_TTC/DATA bits are defined to provide TTC information as well as initialization functions (Aurora). The TTC information is sourced from a dedicated TTC interface on the HUB module.

- Feature to transmit the Reset signal (Aurora Initialization) from the Readout_CTRL link and distribute it to the appropriate shelf slot.

- Several links Combined_TTC links within the shelf; each FEX slot (3-14) and each HUB; one between each HUB and ROD; links between two HUBs.

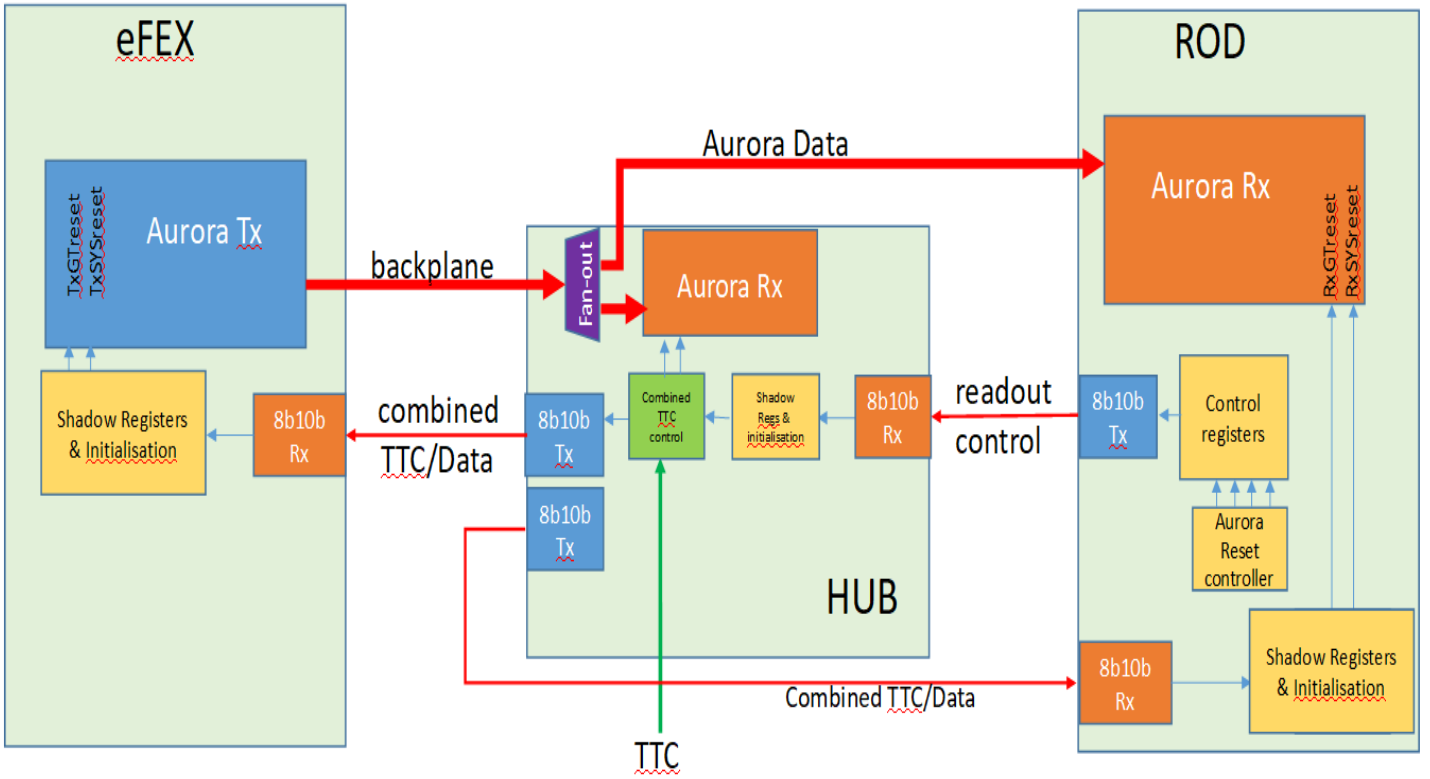
- Combined_TTC/DATA links on the HUB FPGA will be implemented with use of several components, including the MGT transceivers (GTH and GTY), control and diagnostic logic.

- Implementation assumes 4 Control Registers on the HUB TX side and the Shadow Register on the RX side. Transmitter side generates the 128 bit word from 4 Control Registers:

  - Transmitter side logic is in charge to write control information into these Control Registers
  - Contents of these registers are transmitted to the modules which receives the data into a duplicate set of 4 Shadow Registers.
  - Anything written into a Control Register at the transmitter side will appear in the Shadow Register at the receiving side (within the following LHC clock).

Combined_TTC/DATA overview

Ed's diagram



Full spec at: Specification for Readout Control & Combined TTC Serial links in L1Calo

Control and Shadow Register overview

There are Control Registers on the TX side and Shadow Register on the RX side.

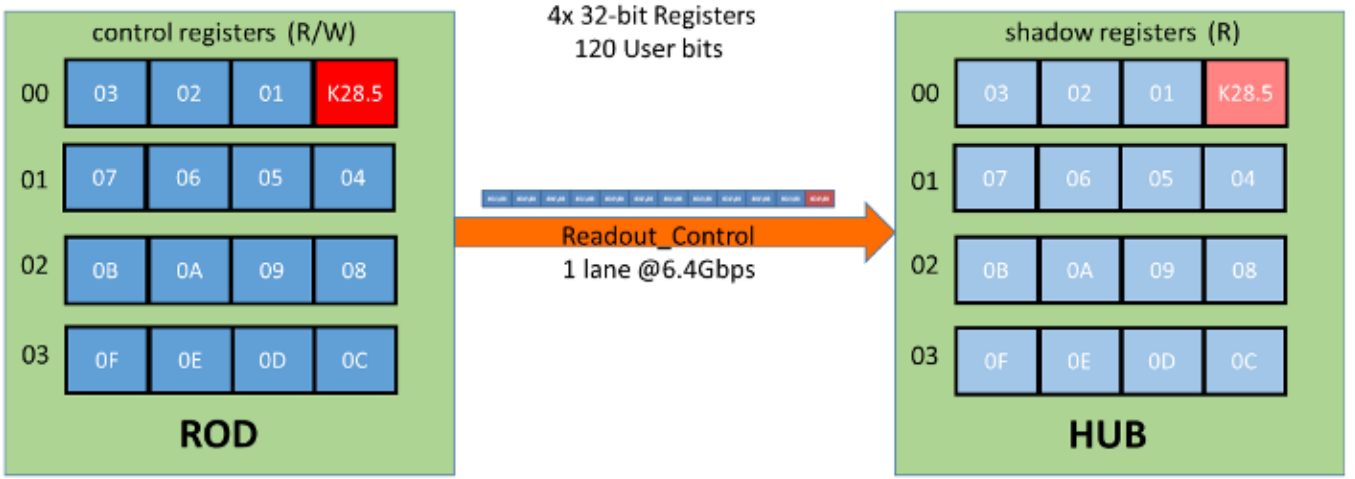


Figure 1: Control and Shadow Registers

Full spec at: Specification for Readout Control & Combined TTC Serial links in L1Calo

Combined_TTC/DATA overview

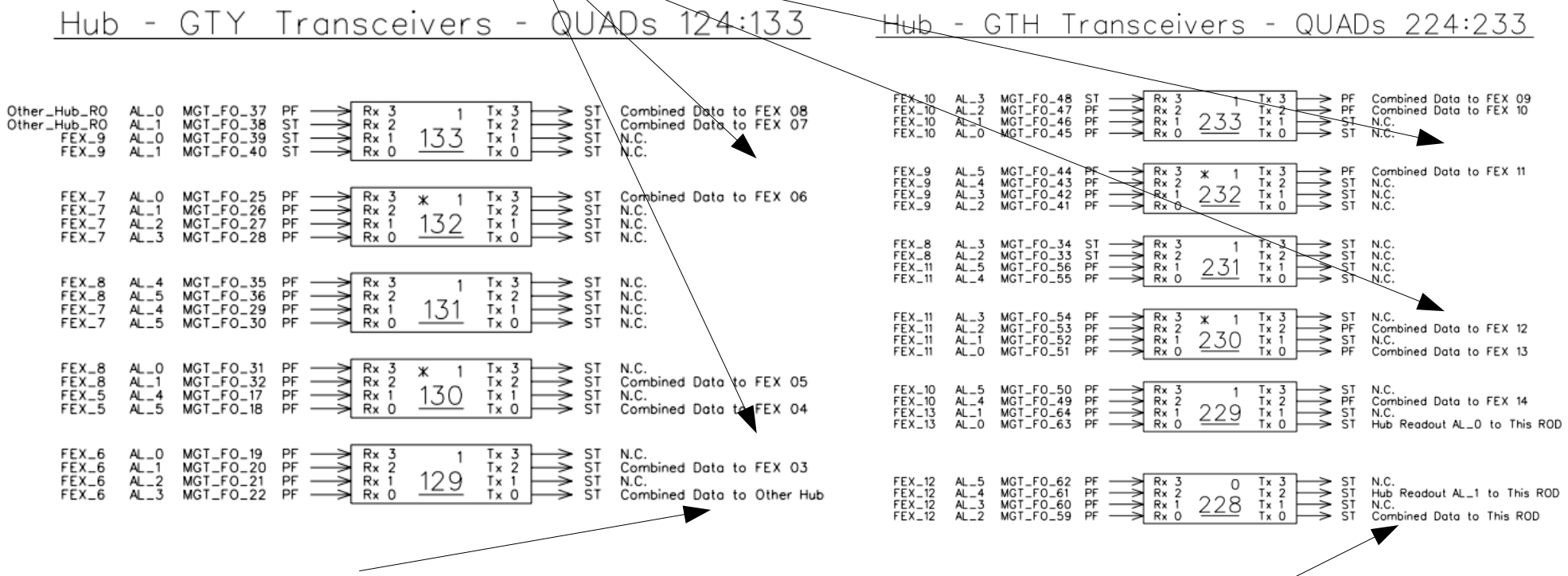
Combined_TTC/DATA bit definitions:

word 0		word 1		word 2		word 3	
bit	0XBC= K28.5	bit		bit		bit	
0	0	0	L1ID	0	control channel	0	Link reset 0
1	0	1	L1ID	1	control channel	1	Link reset 1
2	1	2	L1ID	2	control channel	2	Link reset 2
3	1	3	L1ID	3	control channel	3	Link reset 3
4	1	4	L1ID	4	control channel	4	ROD Busy
5	1	5	L1ID	5	control channel	5	Link Enable
6	0	6	L1ID	6	control channel	6	0 (ROD reserved)
7	1	7	L1ID	7	control channel	7	0 (ROD reserved)
8	version[0]	8	L1ID	8	control channel	8	0 (ROD reserved)
9	version[1]	9	L1ID	9	control channel	9	0 (ROD reserved)
10	version[2]	10	L1ID	10	control channel	10	0 (ROD reserved)
11	version[3]	11	L1ID	11	control channel	11	0 (ROD reserved)
12	reset	12	L1ID	12	control channel	12	0 (ROD reserved)
13	reset	13	L1ID	13	control channel	13	0 (ROD reserved)
14	reset	14	L1ID	14	control channel	14	0 (ROD reserved)
15	reset	15	L1ID	15	control channel	15	0 (ROD reserved)
16	L1A	16	L1ID	16	control channel	16	0 (ROD reserved)
17	BCR	17	L1ID	17	control channel	17	0 (ROD reserved)
18	ECR	18	L1ID	18	control channel	18	0 (ROD reserved)
19	0 (TTC reserved)	19	L1ID	19	control channel	19	0 (ROD reserved)
20	0 (TTC reserved)	20	L1ID	20	control channel	20	shelf #
21	0 (TTC reserved)	21	L1ID	21	control channel	21	shelf #
22	0 (TTC reserved)	22	L1ID	22	control channel	22	shelf #
23	0 (TTC reserved)	23	L1ID	23	control channel	23	CRC (9-bit)
24	0 (TTC reserved)	24	reserved	24	control channel	24	CRC (9-bit)
25	0 (TTC reserved)	25	reserved	25	control channel	25	CRC (9-bit)
26	0 (TTC reserved)	26	reserved	26	control channel	26	CRC (9-bit)
27	0 (TTC reserved)	27	reserved	27	control channel	27	CRC (9-bit)
28	0 (TTC reserved)	28	reserved	28	control channel	28	CRC (9-bit)
29	0 (TTC reserved)	29	reserved	29	control channel	29	CRC (9-bit)
30	0 (TTC reserved)	30	reserved	30	control channel	30	CRC (9-bit)
31	0 (TTC reserved)	31	reserved	31	control channel	31	CRC (9-bit)

Full spec at: Specification for Readout Control & Combined TTC Serial links in L1Calo

HUB FPGA
Combined_TTC/DATA links placement

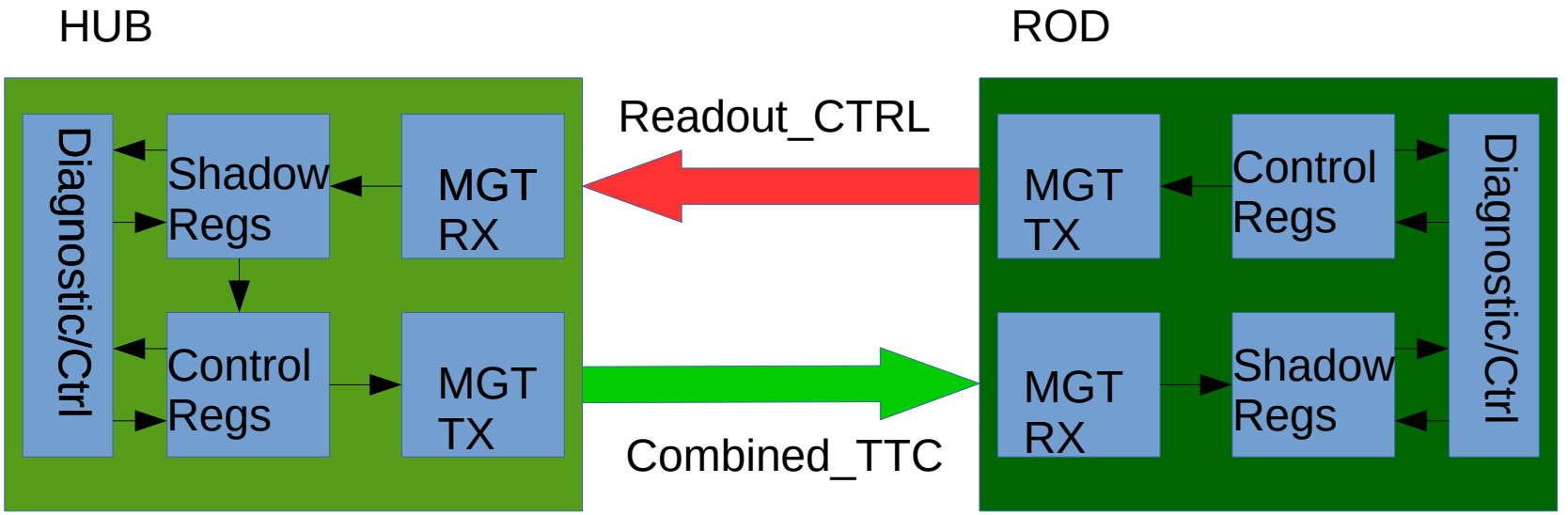
Links between each FEX slot and HUB



Link between two HUBs

Link between the ROD and HUB

Combined_TTC/DATA and Readout_CTRL FW development scheme



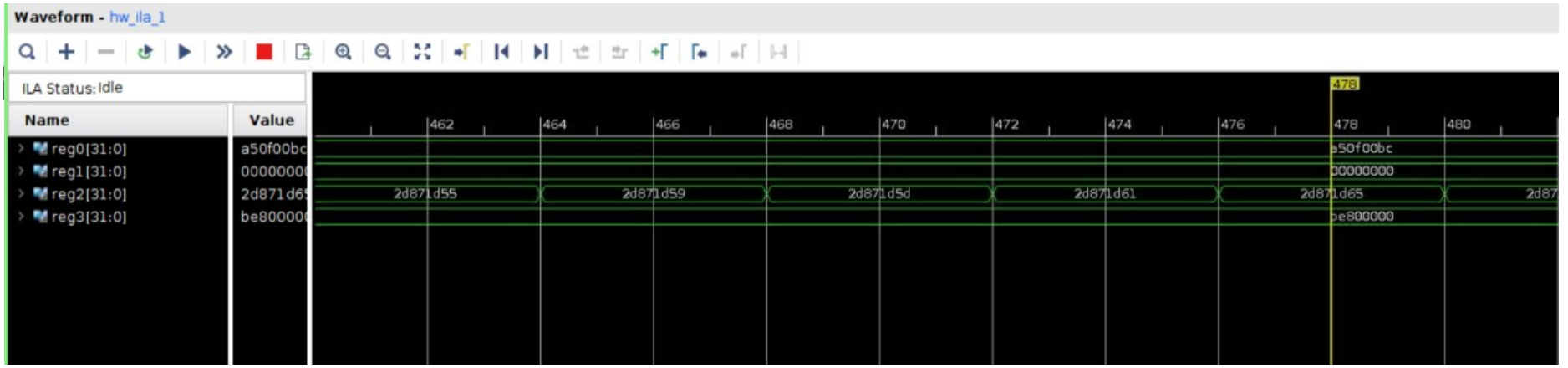
- FW development comprises several stages
- Readout_CTRL link from the ROD (done)
- Combined_TTC/DATA link to the ROD (tests in progress)
- Static patterns will be replaced by real TTC component
- Next modules (receivers) will be added gradually

Readout_CTRL link (ROD & HUB)

Probing the aligned data from the GT

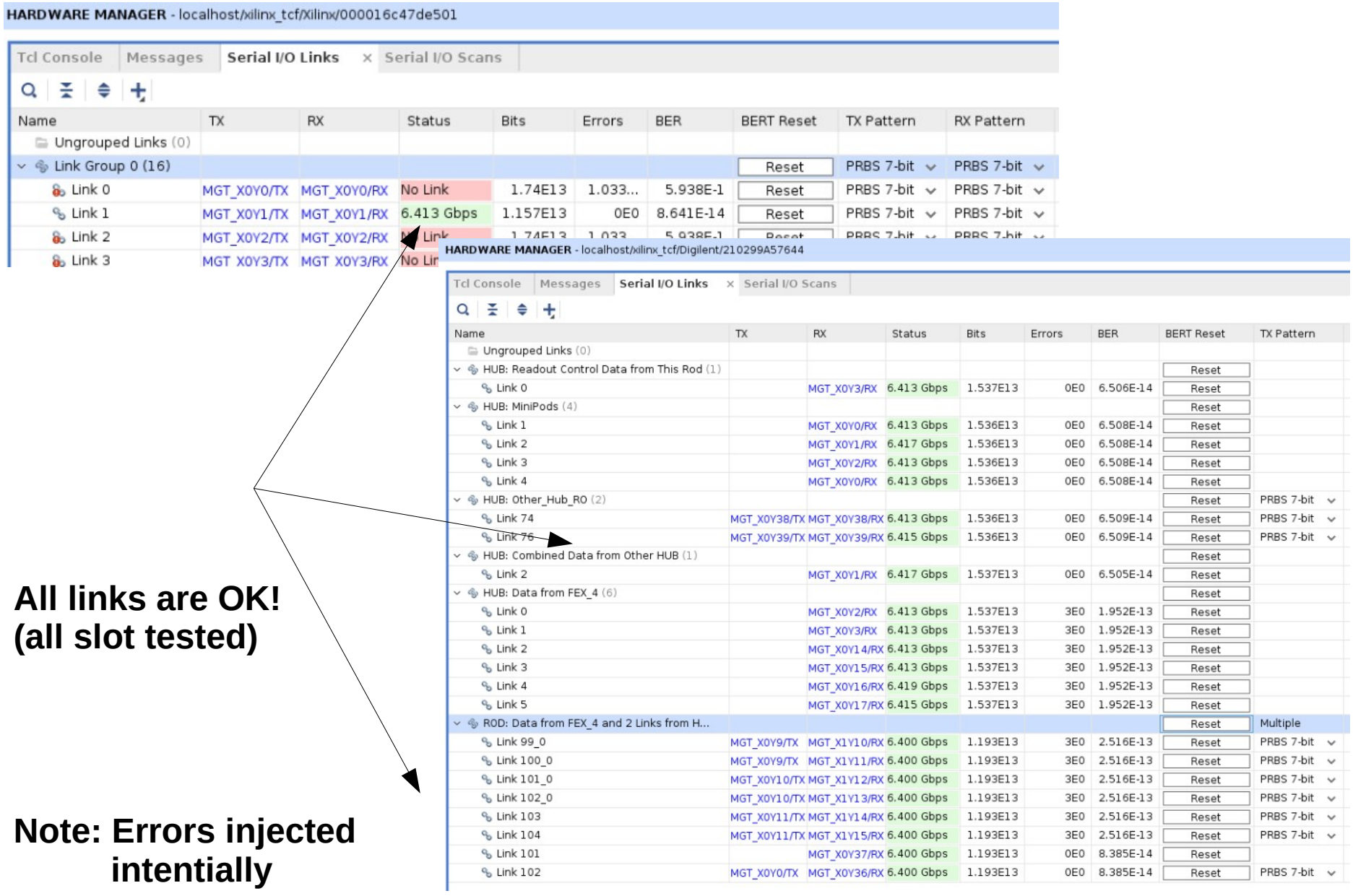
Expected Results
Word_0: constant a50f00bc
Word_1: constant 00000000
Word_2: counter value
Word_3: constant be800000

HUB, It works!



Physical implementation of the Readout_CTRL link is similar to the Combined_TTC links. There are Control Registers on the TX side and Shadow Register on the RX side.

Combined_TTC/DATA link test (IBERT)



HARDWARE MANAGER - localhost/xilinx_tcf/Xilinx/000016c47de501

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (16)							Reset	PRBS 7-bit	PRBS 7-bit
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	No Link	1.74E13	1.033...	5.938E-1	Reset	PRBS 7-bit	PRBS 7-bit
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	6.413 Gbps	1.157E13	0E0	8.641E-14	Reset	PRBS 7-bit	PRBS 7-bit
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	No Link	1.74E13	1.033	5.938E-1	Reset	PRBS 7-bit	PRBS 7-bit
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	No Lir						

HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210299A57644

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern
Ungrouped Links (0)								
HUB: Readout Control Data from This Rod (1)							Reset	
Link 0		MGT_X0Y3/RX	6.413 Gbps	1.537E13	0E0	6.506E-14	Reset	
HUB: MiniPods (4)							Reset	
Link 1		MGT_X0Y0/RX	6.413 Gbps	1.536E13	0E0	6.508E-14	Reset	
Link 2		MGT_X0Y1/RX	6.417 Gbps	1.536E13	0E0	6.508E-14	Reset	
Link 3		MGT_X0Y2/RX	6.413 Gbps	1.536E13	0E0	6.508E-14	Reset	
Link 4		MGT_X0Y0/RX	6.413 Gbps	1.536E13	0E0	6.508E-14	Reset	
HUB: Other_Hub_RO (2)							Reset	PRBS 7-bit
Link 74	MGT_X0Y38/TX	MGT_X0Y38/RX	6.413 Gbps	1.536E13	0E0	6.509E-14	Reset	PRBS 7-bit
Link 76	MGT_X0Y39/TX	MGT_X0Y39/RX	6.415 Gbps	1.536E13	0E0	6.509E-14	Reset	PRBS 7-bit
HUB: Combined Data from Other HUB (1)							Reset	
Link 2		MGT_X0Y1/RX	6.417 Gbps	1.537E13	0E0	6.505E-14	Reset	
HUB: Data from FEX_4 (6)							Reset	
Link 0		MGT_X0Y2/RX	6.413 Gbps	1.537E13	3E0	1.952E-13	Reset	
Link 1		MGT_X0Y3/RX	6.413 Gbps	1.537E13	3E0	1.952E-13	Reset	
Link 2		MGT_X0Y14/RX	6.413 Gbps	1.537E13	3E0	1.952E-13	Reset	
Link 3		MGT_X0Y15/RX	6.413 Gbps	1.537E13	3E0	1.952E-13	Reset	
Link 4		MGT_X0Y16/RX	6.419 Gbps	1.537E13	3E0	1.952E-13	Reset	
Link 5		MGT_X0Y17/RX	6.415 Gbps	1.537E13	3E0	1.952E-13	Reset	
ROD: Data from FEX_4 and 2 Links from H...							Reset	Multiple
Link 99_0	MGT_X0Y9/TX	MGT_X1Y10/RX	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PRBS 7-bit
Link 100_0	MGT_X0Y9/TX	MGT_X1Y11/RX	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PRBS 7-bit
Link 101_0	MGT_X0Y10/TX	MGT_X1Y12/RX	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PRBS 7-bit
Link 102_0	MGT_X0Y10/TX	MGT_X1Y13/RX	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PRBS 7-bit
Link 103	MGT_X0Y11/TX	MGT_X1Y14/RX	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PRBS 7-bit
Link 104	MGT_X0Y11/TX	MGT_X1Y15/RX	6.400 Gbps	1.193E13	3E0	2.516E-13	Reset	PRBS 7-bit
Link 101		MGT_X0Y37/RX	6.400 Gbps	1.193E13	0E0	8.385E-14	Reset	
Link 102	MGT_X0Y0/TX	MGT_X0Y36/RX	6.400 Gbps	1.193E13	0E0	8.385E-14	Reset	PRBS 7-bit

All links are OK!
(all slot tested)

Note: Errors injected intentially

Summary

- ROD → HUB: Readout Control link implemented&tested
- Combined TTC/Data link to the ROD implemented (tests ongoing)
- TTC test pattern will be replaced by real TTC data
- Next receiver → eFEX slot 3
- Adding more receivers → will be done gradually
- FW development scheme needs to be discussed