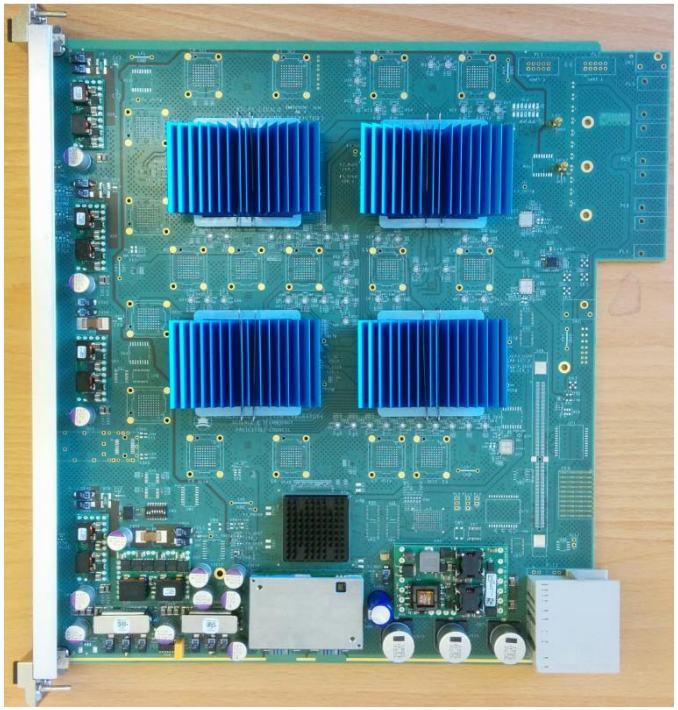
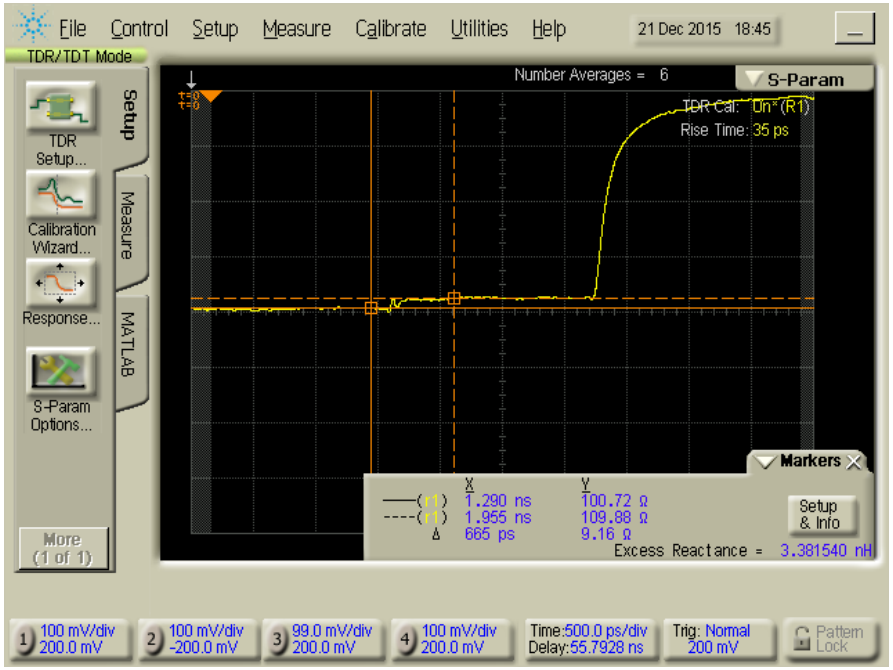
eFEX status

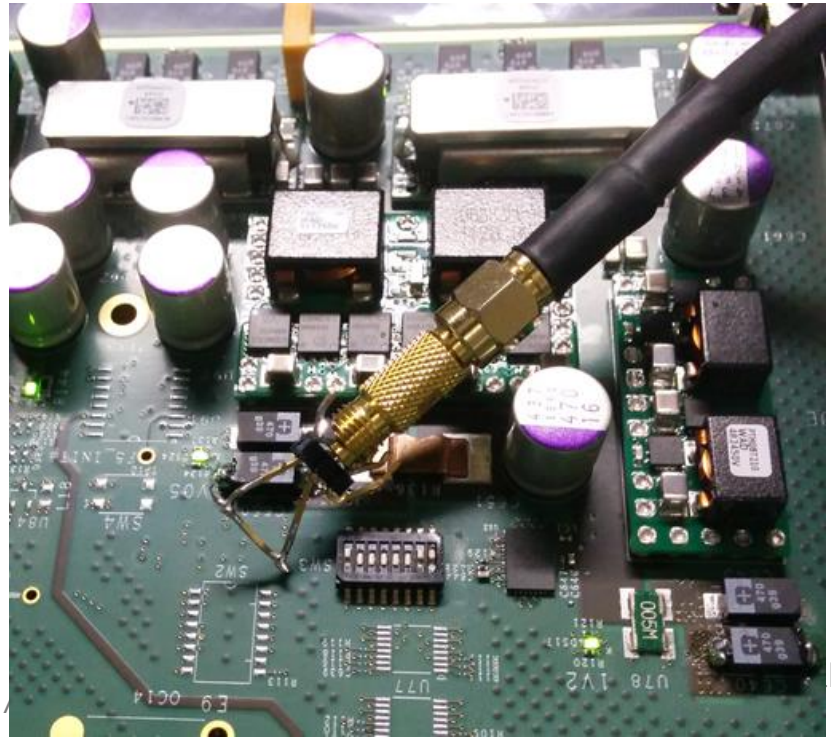
- eFEX PCB
  - 3 PCBs delivered by Invotech by the end of 1025
  - 1 PCB was double checked at RAL and passed impedance tests
  - 1 PCB is being assembled by Jaltek
    - Delivery next week
  - 1 Partial assembled board with power circuitry
    - Use the borderline PCB of 1st batch

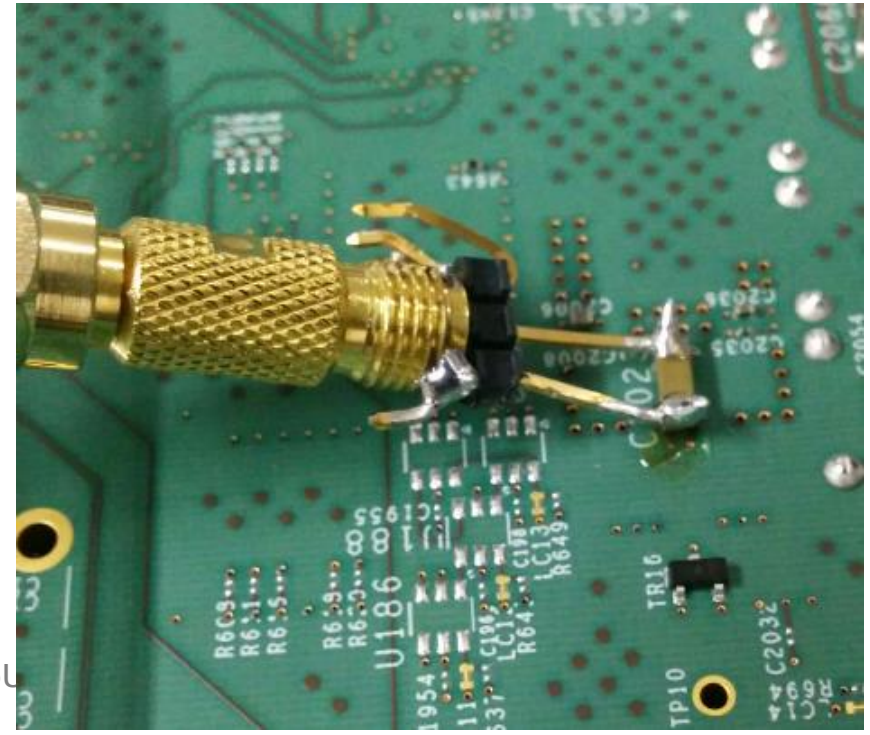




eFEX power investigation

- All power rails came up with correct DC voltages!
- Noise performance
  - Xilinx MGT requirement: ~10mV Max.
  - Tricky to measure the noise with high accuracy
    - EMI pickup ~100mV with Loop area ~ half cm^^2
  - Noise measured at bottom side across a ceramic capacitor is ~10mV





eFEX firmware

- Link speed test A
  - All IBERT cores are generated for both processor FPGAs and control FPGAs
  - 6.4Gbps, 9.6Gbps and 11.2Gbps
  - IPBus firmware for control FPGA to set up clocking scheme
    - System clock selection: local vs backplane
    - Clock PLL (CDCE62005) settings
  - Ready for eFEX hardware lab test in next week
- Link speed test B
  - Adapt LAr link speed test engine firmware
  - IPBus firmware for processor FPGAs
    - IPBus communication between Control FPGA and processor FPGAs
  - Will be ready by the beginning of Feb16