E61 Electronics Overview

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Introduction

The photosensors for E61 will be mPMT modules which contain a cluster of nineteen 3" diameter inner detector PMTs and seven 3" diameter outer detector (OD) PMTs, encapsulated in an acrylic pressure vessel. This style of photosensor was inspired by the KM3NeT mPMT optical module and ongoing mPMT candidates for IceCube-Gen2 and Hyper-K. A diagram of an mPMT can be seen in Figure 1.

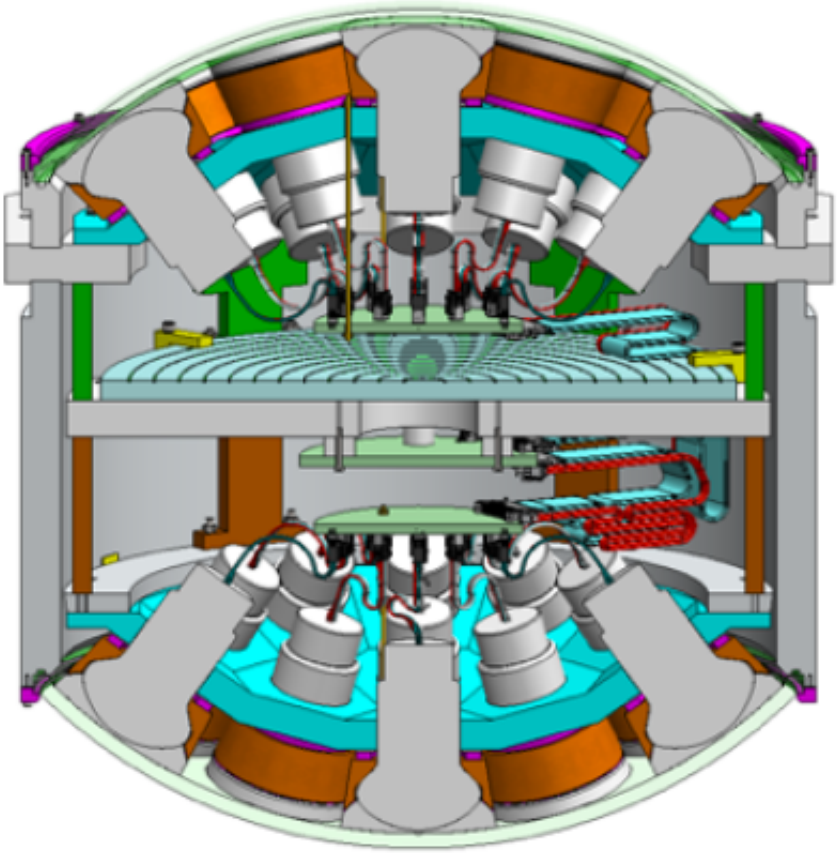

Figure 1: mPMT layout. 19 PMTs face inwards and 7 PMTs face outwards. Digitizing electronics sit on the circular pale blue disks at the center of the module. The module is water-tight, with a cylindrical aluminum body with acrylic domes at the ends.

For the mPMT we require low power and low cost electronics (given the channel count). The digitizing electronics will be contained within the mPMT, so that only digital data will be sent out of the mPMT. All the electronics components also share the common requirements of extreme long-term reliability; these requirements drive many of the electronics choices. Great

care must be taken in the choice and fabrication of the electronics components. In addition, redundancy in the circuit design, in particular in the power supply and low-level functions, is essential. Where possible, we will build on experience from the KM3NET and ICECUBE groups in developing electronics for similar applications.

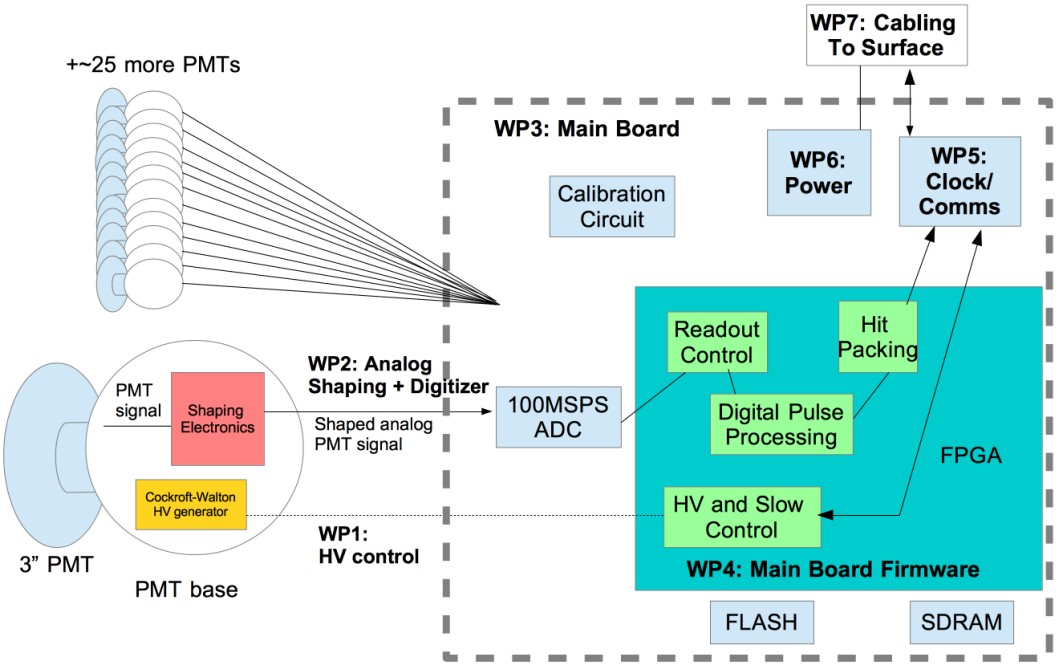

Figure 2: block diagram of mPMT electronics, with proposed work packages.

The block diagram for the proposed mPMT electronics is shown in Figure 2. The basic concept is as follows:

- We generate the PMT HV on the PMT base using a Cockroft-Walton circuit.
- PMT signals are shaped and then digitized with 100MSPS or 200MSPS ADC on the mainboard.
- Digitized PMT signals are processed with digital pulse processing algorithms in the mainboard FPGA. Algorithms will find PMT pulses above threshold and save relevant information for each pulse.
- PMT pulse information gets packetized and then sent over link to the backend computers.

The following are some details about the key electronics components. The electronics has been split into proposed work packages (WP).

WP1: PMT HV

Goal: provide configurable HV for each PMT using Cockroft-Walton circuit.

Requirements:

- PMT HV set between 750V and 1750V (??)
- PMT HV stable to 0.2% level (??) - (rough specification – will be revised once charge resolution of PMTs is measured)
- HV ripple < 50 mVpp (to be confirmed after PMT characterization)

Implementation details: we envision that the HV will be controlled by uC either on PMT base or on mainboard. Not clear yet whether to use positive or negative HV for the PMT. We would prefer to use negative voltage, as it does not couple HV ripple into the signal and also provides for a DC coupling (which ensures constant pedestal). However, we need to confirm that it is feasible given the expected increase in dark rate due to photocathode at high potential.

WP status: KM3NET and ICECUBE have functioning designs for this component that should make development of these circuits easy. Italian group already working on prototype. Believe that between Italian and Warsaw groups this work can be covered.

WP2: PMT Signal Analog Electronics

Goal: shape PMT signals in order to achieve optimal timing and charge resolution with cheap, low-power 100-200MSPS ADC.

Requirements:

- Timing resolution: ≤0.5ns timing resolution (FWHM) for electronics for single PE pulse.
- Charge resolution ~0.05PE up to 25PE.
- Charge dynamic range 0.1PE – 100PE
- Deadtime-less at electronics level, but will probably provide global triggers to reduce data rate to DAQ.
- Able to resolve pulses in different bunchs (600ns bunch separation) and maybe within bunch (25ns bunch width)
- Minimize power; the overall goal for mPMT is for power to be <10W per mPMT (hopefully <5W).

Implementation details: we have done simulation and bench-top tests that suggest that we can achieve the above requirements using 100-200MSPS ADC. Exact performance depends on the details of the digital pulse processing algorithms in firmware.

WP status: Warsaw and TRIUMF groups have been working on the techniques for this WP; we envision that Warsaw will do board layout.

WP3: Mainboard Design

Goal: do main layout for mainboard including FPGA, microcontrollers, memory, environment monitoring, etc

Requirements:

- Board dimensions must fit within mechanically constraints of mPMT. Diameter of circular mainboard is ~14-16inches
- Minimize power; the overall goal for mPMT is for power to be <10W (hopefully <5W).
- Careful layout of all clock lines and digital signals, ensuring minimum emissions of EMI. It is extremely important, as PMT tend to be relatively good antennas.
- Some investigation of shielding and EMI emissions may be necessary. WUT may help with that.
- Need to pay attention to thermals (i.e. connection of ICs to case for efficient cooling).

Implementation details: for initial prototypes we can imagine having mezzanine cards to provide the functionality of other work packages (namely WP1,2,5,6) so that we can more efficiently divide up the work.

WP Status: not really started; may find TRIUMF manpower to work on this; we have a similar digitizer (in VME form factor) that we could start from. But the prospect for this project is unclear.

WP4: Mainboard Firmware

Goal: provide the main firmware algorithms for controlling the board, including controlling digitization, pulse processing, memory management and interfacing with communication.

Requirements:

- Control the fast ADC digitization.
- Apply digital pulse processing
- Control memory management
- Interface with communication block
- Slow control monitoring (including interface to PMT HV control)
- Design firmware for low power – investigate smart clock management.

Implementation details: WUT firmware group has substantial experience with different pulse processing algorithms and compression techniques, which will probably be applicable.

WP Status: probably WUT group will lead this work.

WP5: Clock and Communication

Goal: provide clock and communication to the mainboard.

Requirements:

- Probably need 1Gb/s communication speed, though 100Mb/s might suffice.
- Need clock that is stable enough for accurate 100ps timing of PMT hits.

Implementation details: QMUL group has been investigating the White Rabbit clock/communication scheme used by CERN and KM3NET. This seems like it might work well for E61.

WP Status: ???

WP6: Power

Goal: provide stable power to the mPMT electronics.

Requirements:

- Low EMI, high efficiency switching power supplies.
- Probably shielding will be necessary to control EMI.

Implementation details: we envision sending 48V or 50V down the cables and down-converting to lower voltages on the mainboard.

WP Status: ???

WP7: Cabling

Goal: need to figure out sort of cables to use surface.

Requirements:

- Cables must be water-tight, down to ~100m of water depth.
- Cables provide power and communication
- It would be good to consider whether there can be power distribution units on the E61 detector, so that we can minimize the number of long cables that must be spooled up as E61 detector moves up and down.

Implementation details: The cable choice will be coupled to the choice of penetrator. The cable choice will be coupled to the choice of power distribution and clock/communication scheme.

WP Status: ???