## 15.4 Emitter-Coupled Logic (ECL)

Emitter-coupled logic (ECL) is the fastest logic circuit family available for conventional logic-system design.[4] High speed is achieved by operating all bipolar transistors out of saturation, thus avoiding storage-time delays, and by keeping the logic signal swings relatively small (about 0.8 V or less), thus reducing the time required to charge and discharge the various load and parasitic capacitances. Saturation in ECL is avoided by using the BJT differential pair as a current switch.[5] The BJT differential pair was studied in Chapter 9, and we urge the reader to review the introduction given in Section 9.2 before proceeding with the study of ECL.

### 15.4.1 The Basic Principle

Emitter-coupled logic is based on the use of the current-steering switch introduced in Section 15.6. Such a switch can be most conveniently realized using the differential pair shown in Fig. 15.25. The pair is biased with a constant-current source $I$, and one side is connected to a reference voltage $V_R$. As shown in Section 9.2, the current $I$ can be steered to either $Q_1$ or $Q_2$ under the control of the input signal $v_I$. Specifically, when $v_I$ is greater than $V_R$ by about $4V_T$ ($\simeq$100 mV), nearly all the current $I$ is conducted by $Q_1$, and thus for $\alpha_1 \simeq 1$, $v_{O1} = V_{CC} - IR_C$. Simultaneously, the current through $Q_2$ will be nearly zero, and thus $v_{O2} = V_{CC}$. Conversely, when $v_I$ is lower than $V_R$ by about $4V_T$, most of the current $I$ will flow through $Q_2$ and the current through $Q_1$ will be nearly zero. Thus $v_{O1} = V_{CC}$ and $v_{O2} = V_{CC} - IR_C$.

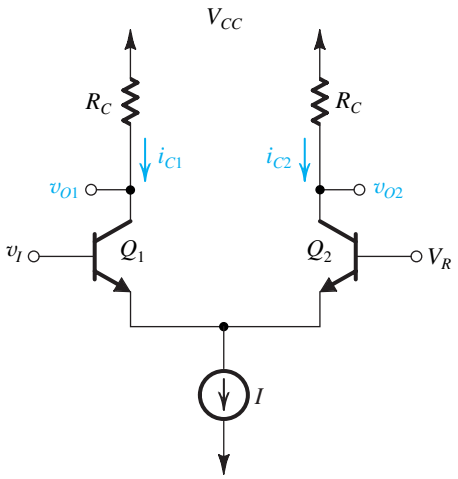


**Figure 15.25** The basic element of ECL is the differential pair. Here, $V_R$ is a reference voltage.

[4] Although higher speeds of operation can be obtained with gallium arsenide (GaAs) circuits, the latter are not available as off-the-shelf components for conventional digital system design. GaAs digital circuits are not covered in this book; however, a substantial amount of material on this subject can be found on the disc accompanying the book and on the website.

[5] This is in sharp contrast to the technique utilized in a nonsaturating variant of transistor-transistor logic (TTL) known as Schottky TTL. There, a Schottky diode is placed across the CBJ junction to shunt away some of the base current and, owing to the low voltage drop of the Schottky diode, the CBJ is prevented from becoming forward biased.

The preceding description suggests that as a logic element, the differential pair realizes an inversion function at $v_{O1}$ and simultaneously provides the complementary output signal at $v_{O2}$. The output logic levels are $V_{OH} = V_{CC}$ and $V_{OL} = V_{CC} - IR_C$, and thus the output logic swing is $IR_C$. A number of additional remarks can be made concerning this circuit:

1. The differential nature of the circuit makes it less susceptible to picked-up noise. In particular, an interfering signal will tend to affect both sides of the differential pair similarly and thus will not result in current switching. This is the common-mode rejection property of the differential pair (see Section 9.2).
2. The current drawn from the power supply remains constant during switching. Thus, unlike CMOS (and TTL), no supply current spikes occur in ECL, eliminating an important source of noise in digital circuits. This is a definite advantage, especially since ECL is usually designed to operate with small signal swings and has correspondingly low noise margins.
3. The output signal levels are both referenced to $V_{CC}$ and thus can be made particularly stable by operating the circuit with $V_{CC} = 0$: in other words, by utilizing a negative power supply and connecting the $V_{CC}$ line to ground. In this case, $V_{OH} = 0$ and $V_{OL} = -IR_C$.
4. Some means must be provided to make the output signal levels compatible with those at the input so that one gate can drive another. As we shall see shortly, practical ECL gate circuits incorporate a level-shifting arrangement that serves to center the output signal levels on the value of $V_R$.
5. The availability of complementary outputs considerably simplifies logic design with ECL.

**EXERCISE**

**15.11** For the circuit in Fig. 15.25, let $V_{CC} = 0$, $I = 4$ mA, $R_C = 220\,\Omega$, $V_R = -1.32$ V, and assume $\alpha \simeq 1$. Determine $V_{OH}$ and $V_{OL}$. By how much should the output levels be shifted so that the values of $V_{OH}$ and $V_{OL}$ become centered on $V_R$? What will the shifted values of $V_{OH}$ and $V_{OL}$ be?
**Ans.** 0; –0.88 V; –0.88 V; –0.88 V, –1.76 V

## 15.4.2 ECL Families

Currently there are two popular forms of commercially available ECL—namely, ECL 10K and ECL 100K. The ECL 100K series features gate delays on the order of 0.75 ns and dissipates about 40 mW/gate, for a delay–power product of 30 pJ. Although its power dissipation is relatively high, the 100K series provides the shortest available gate delay in small- and medium-scale integrated circuit packages.

The ECL 10 K series is slightly slower; it features a gate propagation delay of 2 ns and a power dissipation of 25 mW for a delay–power product of 50 pJ. Although the value of *PDP* is higher than that obtained in the 100K series, the 10K series is easier to use. This is because the rise and fall times of the pulse signals are deliberately made longer, thus reducing signal coupling, or cross talk, between adjacent signal lines. ECL 10K has an "edge speed"

of about 3.5 ns, compared with the approximately 1 ns of ECL 100K. To give concreteness to our study of ECL, in the following we shall consider the popular ECL 10K in some detail. The same techniques, however, can be applied to other types of ECL.

In addition to its usage in SSI and MSI circuit packages, ECL is also employed in large-scale and VLSI applications. A variant of ECL known as **current-mode logic** (CML) is utilized in VLSI applications (see Treadway, 1989, and Wilson, 1990).

### 15.4.3 The Basic Gate Circuit

The basic gate circuit of the ECL 10K family is shown in Fig. 15.26. The circuit consists of three parts. The network composed of $Q_1$, $D_1$, $D_2$, $R_1$, $R_2$, and $R_3$ generates a reference voltage $V_R$ whose value at room temperature is –1.32 V. As will be shown, the value of this reference voltage is made to change with temperature in a predetermined manner to keep the noise margins almost constant. Also, the reference voltage $V_R$ is made relatively insensitive to variations in the power-supply voltage $V_{EE}$.

**EXERCISE**

**15.12** Figure E15.12 shows the circuit that generates the reference voltage $V_R$. Assuming that the voltage drop across each of $D_1$, $D_2$, and the base–emitter junction of $Q_1$ is 0.75 V, calculate the value of $V_R$. Neglect the base current of $Q_1$.

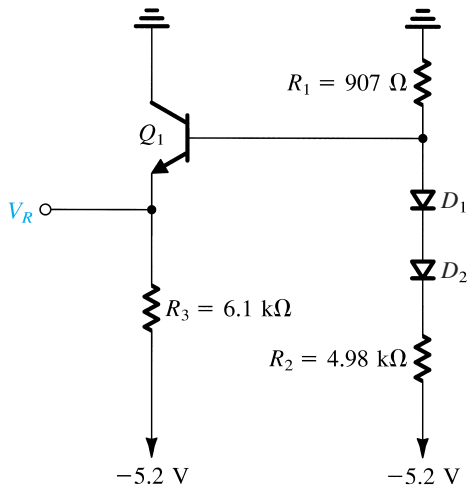


**Figure E15.12**

**Ans.** –1.32 V

The second part, and the heart of the gate, is the differential amplifier formed by $Q_R$ and either $Q_A$ or $Q_B$. This differential amplifier is biased not by a constant-current source, as was done in the circuit of Fig. 15.25, but with a resistance $R_E$ connected to the negative supply $-V_{EE}$. Nevertheless, we will shortly show that the current in $R_E$ remains approximately

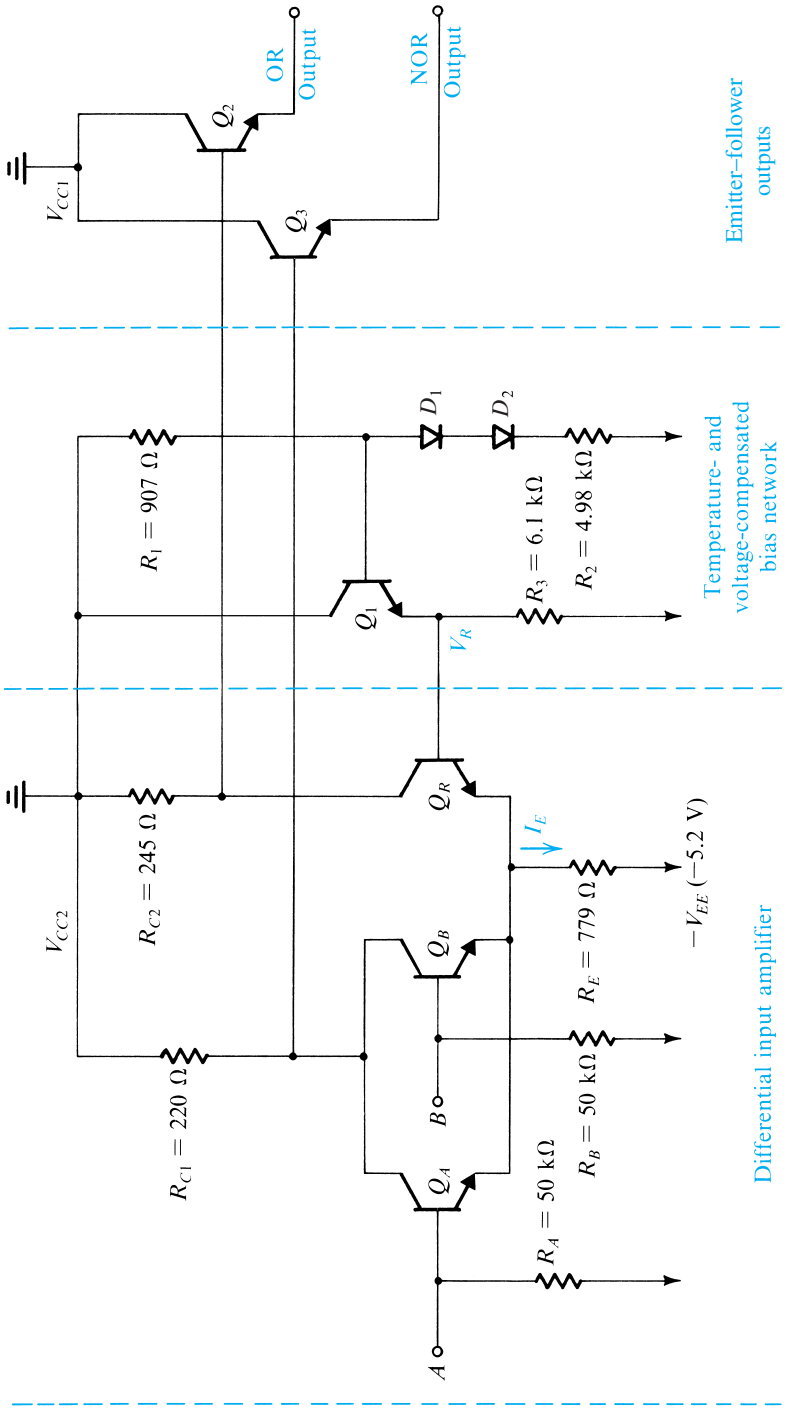


**Figure 15.26** Basic circuit of the ECL 10K logic-gate family.

constant over the normal range of operation of the gate. One side of the differential amplifier consists of the reference transistor $Q_R$, whose base is connected to the reference voltage $V_R$. The other side consists of a number of transistors (two in the case shown), connected in parallel, with separated bases, each connected to a gate input. If the voltages applied to $A$ and $B$ are at the logic-0 level, which, as we will soon find out, is about 0.4 V below $V_R$, both $Q_A$ and $Q_B$, will be off and the current $I_E$ in $R_E$ will flow through the reference transistor $Q_R$. The resulting voltage drop across $R_{C2}$ will cause the collector voltage of $Q_R$ to be low.

On the other hand, when the voltage applied to $A$ or $B$ is at the logic-1 level, which, as we will show shortly, is about 0.4 V above $V_R$, transistor $Q_A$ or $Q_B$, or both, will be on and $Q_R$ will be off. Thus the current $I_E$ will flow through $Q_A$ or $Q_B$, or both, and an almost equal current will flow through $R_{C1}$. The resulting voltage drop across $R_{C1}$ will cause the collector voltage to drop. Meanwhile, since $Q_R$ is off, its collector voltage rises. We thus see that the voltage at the collector of $Q_R$ will be high if $A$ or $B$, or both, is high, and thus at the collector of $Q_R$, the OR logic function, $A + B$, is realized. On the other hand, the common collector of $Q_A$ and $Q_B$ will be high only when $A$ and $B$ are simultaneously low. Thus at the common collector of $Q_A$ and $Q_B$, the logic function $\overline{A}\,\overline{B} = \overline{A + B}$ is realized. We therefore conclude that the two-input gate of Fig. 15.26 realizes the OR function and its complement, the NOR function. The availability of complementary outputs is an important advantage of ECL; it simplifies logic design and avoids the use of additional inverters with associated time delay.

It should be noted that the resistance connecting each of the gate input terminals to the negative supply enables the user to leave an unused input terminal open: An open input terminal will be *pulled down* to the negative supply voltage, and its associated transistor will be off.

## EXERCISE

**15.13** With input terminals $A$ and $B$ in Fig. 15.26 left open, find the current $I_E$ through $R_E$. Also find the voltages at the collector of $Q_R$ and at the common collector of the input transistors $Q_A$ and $Q_B$. Use $V_R = -1.32$ V, $V_{BE}$ of $Q_R \simeq 0.75$ V, and assume that $\beta$ of $Q_R$ is very high.
**Ans.** 4 mA; –1 V; 0 V

The third part of the ECL gate circuit is composed of the two emitter followers, $Q_2$ and $Q_3$. The emitter followers do not have on-chip loads, since in many applications of high-speed logic circuits the gate output drives a transmission line terminated at the other end, as indicated in Fig. 15.27. (More on this later in Section 15.4.6.)

The emitter followers have two purposes: First, they shift the level of the output signals by one $V_{BE}$ drop. Thus, using the results of Exercise 15.13, we see that the output levels become approximately –1.75 V and –0.75 V. These shifted levels are centered approximately around the reference voltage ($V_R = -1.32$ V), which means that one gate can drive another. This compatibility of logic levels at input and output is an essential requirement in the design of gate circuits.

The second function of the output emitter followers is to provide the gate with low output resistances and with the large output currents required for charging load capacitances. Since these large transient currents can cause spikes on the power-supply line, the collectors of

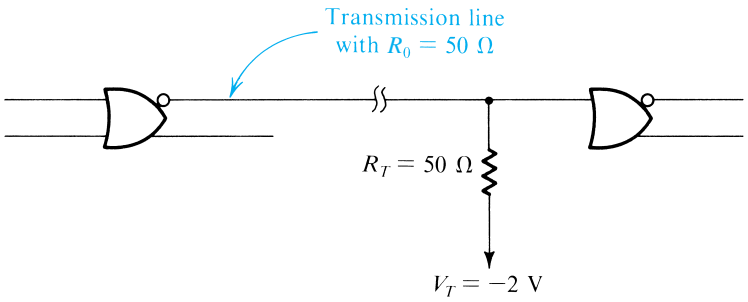


**Figure 15.27** The proper way to connect high-speed logic gates such as ECL. Properly terminating the transmission line connecting the two gates eliminates the "ringing" that would otherwise corrupt the logic signals. (See Section 15.4.6.)

the emitter followers are connected to a power-supply terminal $V_{CC1}$ separate from that of the differential amplifier and the reference-voltage circuit, $V_{CC2}$. Here we note that the supply current of the differential amplifier and the reference circuit remains almost constant. The use of separate power-supply terminals prevents the coupling of power-supply spikes from the output circuit to the gate circuit and thus lessens the likelihood of false gate switching. Both $V_{CC1}$ and $V_{CC2}$ are of course connected to the same system ground, external to the chip.

## 15.4.4 Voltage-Transfer Characteristics

Having provided a qualitative description of the operation of the ECL gate, we shall now derive its voltage-transfer characteristics. This will be done under the conditions that the outputs are terminated in the manner indicated in Fig. 15.27. Assuming that the *B* input is low and thus $Q_B$ is off, the circuit simplifies to that shown in Fig. 15.28. We wish to analyze this circuit to determine $v_{OR}$ versus $v_I$ and $v_{\text{NOR}}$ versus $v_I$ (where $v_I \equiv v_A$).

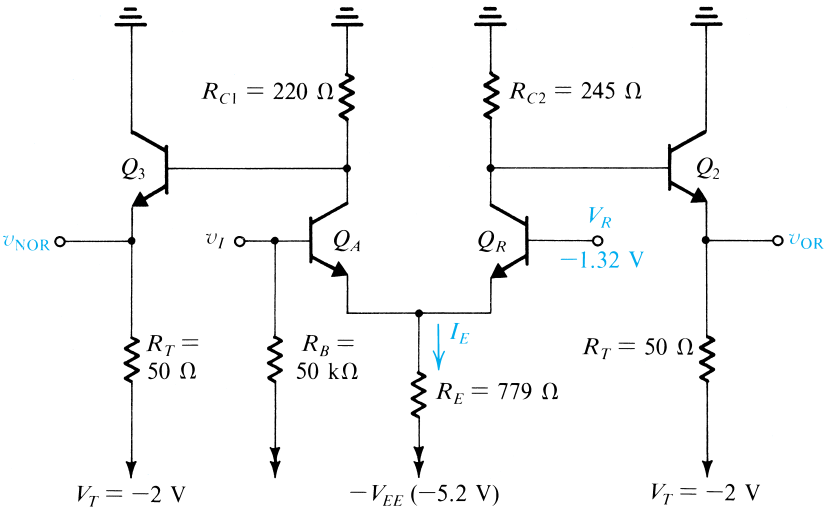


**Figure 15.28** Simplified version of the ECL gate for the purpose of finding transfer characteristics.

In the analysis to follow we shall make use of the exponential $i_C$–$v_{BE}$ characteristic of the BJT. Since the BJTs used in ECL circuits have small areas (in order to have small capacitances and hence high $f_T$), their scale currents $I_S$ are small. We will therefore assume that at an emitter current of 1 mA, an ECL transistor has a $V_{BE}$ drop of 0.75 V.

**The OR Transfer Curve** Figure 15.29 is a sketch of the OR transfer characteristic, $v_{OR}$ versus $v_I$, with the parameters $V_{OL}$, $V_{OH}$, $V_{IL}$, and $V_{IH}$ indicated. However, to simplify the calculation of $V_{IL}$ and $V_{IH}$, we shall use an alternative to the unity-gain definition. Specifically, we shall assume that at point $x$, transistor $Q_A$ is conducting 1% of $I_E$ while $Q_R$ is conducting 99% of $I_E$. The reverse will be assumed for point $y$. Thus at point $x$ we have

$$\frac{I_E\big|_{Q_R}}{I_E\big|_{Q_A}} = 99$$

Using the exponential $i_E$–$v_{BE}$ relationship, we obtain

$$V_{BE}\big|_{Q_R} - V_{BE}\big|_{Q_A} = V_T \ln 99 = 115 \text{ mV}$$

which gives

$$V_{IL} = -1.32 - 0.115 = -1.435 \text{ V}$$

Assuming $Q_A$ and $Q_R$ to be matched, we can write

$$V_{IH} - V_R = V_R - V_{IL}$$

which can be used to find $V_{IH}$ as

$$V_{IH} = -1.205 \text{ V}$$

To obtain $V_{OL}$, we note that $Q_A$ is off and $Q_R$ carries the entire current $I_E$, given by

$$I_E = \frac{V_R - V_{BE}\big|_{Q_R} + V_{EE}}{R_E}$$

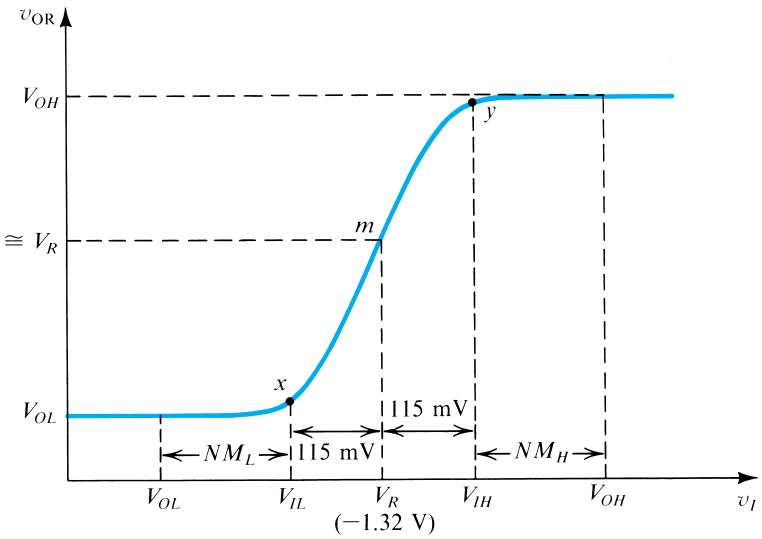


**Figure 15.29** The OR transfer characteristic $v_{OR}$ versus $v_I$, for the circuit in Fig. 15.28.

$$= \frac{-1.32 - 0.75 + 5.2}{0.779}$$

$$\simeq 4 \text{ mA}$$

(If we wish, we can iterate to determine a better estimate of $V_{BE}\big|_{Q_R}$ and hence of $I_E$.) Assuming that $Q_R$ has a high $\beta$ so that its $\alpha \simeq 1$, its collector current will be approximately 4 mA. If we neglect the base current of $Q_2$, we obtain for the collector voltage of $Q_R$

$$V_C\big|_{Q_R} \simeq -4 \times 0.245 = -0.98 \text{ V}$$

Thus a first approximation for the value of the output voltage $V_{OL}$ is

$$V_{OL} = V_C\big|_{Q_R} - V_{BE}\big|_{Q_2}$$
$$\simeq -0.98 - 0.75 = -1.73 \text{ V}$$

We can use this value to find the emitter current of $Q_2$ and then iterate to determine a better estimate of its base–emitter voltage. The result is $V_{BE2} \simeq 0.79$ V and, correspondingly,

$$V_{OL} \simeq -1.77 \text{ V}$$

At this value of output voltage, $Q_2$ supplies a load current of about 4.6 mA.

To find the value of $V_{OH}$ we assume that $Q_R$ is completely cut off (because $v_I > V_{IH}$). Thus the circuit for determining $V_{OH}$ simplifies to that in Fig. 15.30. Analysis of this circuit, assuming $\beta_2 = 100$, results in $V_{BE2} \simeq 0.83$ V, $I_{E2} = 22.4$ mA, and

$$V_{OH} \simeq -0.88 \text{ V}$$

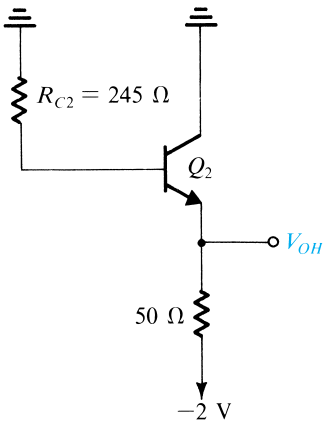


**Figure 15.30** Circuit for determining $V_{OH}$.

## EXERCISE

**15.14** For the circuit in Fig. 15.28, determine the values of $I_E$ obtained when $v_I = V_{IL}$, $V_R$, and $V_{IH}$. Also, find the value of $v_{OR}$ corresponding to $v_I = V_R$. Assume that $v_{BE} = 0.75$ V at a current of 1 mA.
**Ans.** 3.97 mA; 4.00 mA; 4.12 mA; –1.31 V

**Noise Margins** The results of Exercise 15.14 indicate that the bias current $I_E$ remains approximately constant. Also, the output voltage corresponding to $v_I = V_R$ is approximately equal to $V_R$. Notice further that this is also approximately the midpoint of the logic swing; specifically,

$$\frac{V_{OL} + V_{OH}}{2} = -1.325 \simeq V_R$$

Thus the output logic levels are centered around the midpoint of the input transition band. This is an ideal situation from the point of view of noise margins, and it is one of the reasons for selecting the rather arbitrary-looking numbers ($V_R = -1.32$ V and $V_{EE} = 5.2$ V) for reference and supply voltages.

The noise margins can now be evaluated as follows:

$$NM_H = V_{OH} - V_{IH} = -0.88 - (-1.205) = 0.325 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = -1.435 - (-1.77) = 0.335 \text{ V}$$

Note that these values are approximately equal.

**The NOR Transfer Curve** The NOR transfer characteristic, which is $v_{\text{NOR}}$ versus $v_I$ for the circuit in Fig. 15.28, is sketched in Fig. 15.31. The values of $V_{IL}$ and $V_{IH}$ are identical to those found earlier for the OR characteristic. To emphasize this, we have labeled the threshold points $x$ and $y$, the same letters used in Fig. 15.29.

For $v_I < V_{IL}$, $Q_A$ is off and the output voltage $v_{\text{NOR}}$ can be found by analyzing the circuit composed of $R_{C1}$, $Q_3$, and its 50-Ω termination. Except that $R_{C1}$ is slightly smaller than $R_{C2}$, this circuit is identical to that in Fig. 15.30. Thus the output voltage will be only slightly greater than the value $V_{OH}$ found earlier. In the sketch of Fig. 15.31 we have assumed that the output voltage is approximately equal to $V_{OH}$.

For $v_I > V_{IH}$, $Q_A$ is on and is conducting the entire bias current. The circuit then simplifies to that in Fig. 15.32. This circuit can be easily analyzed to obtain $v_{\text{NOR}}$ versus $v_I$ for the range

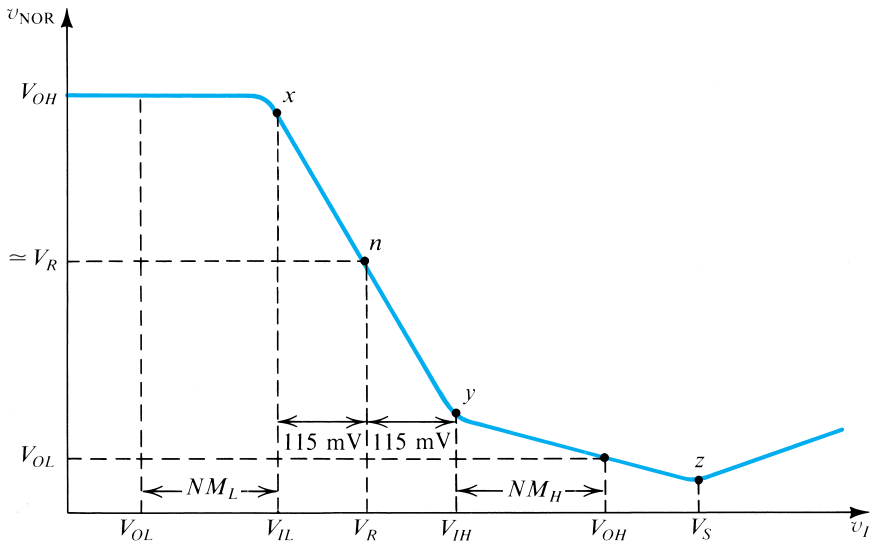


**Figure 15.31** The NOR transfer characteristic, $v_{\text{NOR}}$ versus $v_I$, for the circuit in Fig. 15.28.

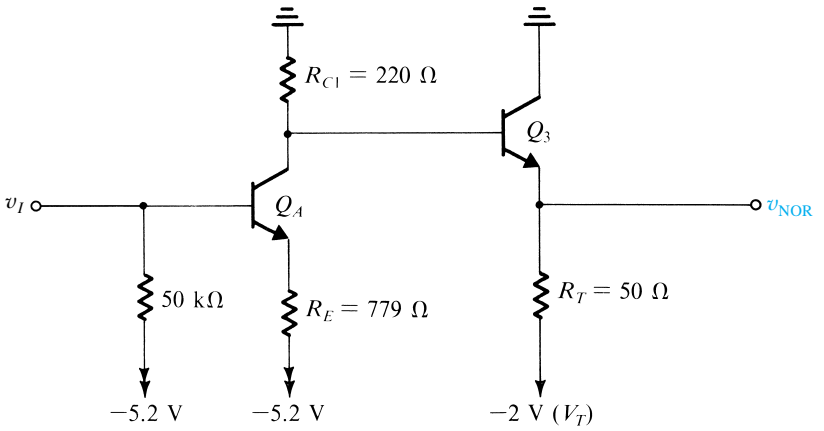


**Figure 15.32** Circuit for finding $v_{NOR}$ versus $v_I$ for the range $v_I > V_{IH}$.

$v_I \geq V_{IH}$. A number of observations are in order. First, note that $v_I = V_{IH}$ results in an output voltage slightly higher than $V_{OL}$. This is because $R_{C1}$ is smaller than $R_{C2}$. In fact, $R_{C1}$ is chosen lower in value than $R_{C2}$ so that with $v_I$ equal to the normal logic-1 value (i.e., $V_{OH}$, which is approximately –0.88 V), the output will be equal to the $V_{OL}$ value found earlier for the OR output.

Second, note that as $v_I$ exceeds $V_{IH}$, transistor $Q_A$ operates in the active mode and the circuit of Fig. 15.32 can be analyzed to find the gain of this amplifier, which is the slope of the segment $yz$ of the transfer characteristic. At point $z$, transistor $Q_A$ saturates. Further increments in $v_I$ (beyond the point $v_I = V_S$) cause the collector voltage and hence $v_{NOR}$ to increase. The slope of the segment of the transfer characteristic beyond point $z$, however, is not unity, but is about 0.5, because as $Q_A$ is driven deeper into saturation, a portion of the increment in $v_I$ appears as an increment in the base–collector forward-bias voltage. The reader is urged to solve Exercise 15.15, which is concerned with the details of the NOR transfer characteristic.

## EXERCISE

**15.15** Consider the circuit in Fig. 15.32. (a) For $v_I = V_{IH} = -1.205$ V, find $v_{NOR}$. (b) For $v_I = V_{OH} = -0.88$ V, find $v_{NOR}$. (c) Find the slope of the transfer characteristic at the point $v_I = V_{OH} = -0.88$ V. (d) Find the value of $v_I$ at which $Q_A$ saturates (i.e., $V_S$). Assume that $V_{BE} = 0.75$ V at a current of 1 mA, $V_{CEsat} \simeq 0.3$ V, and $\beta = 100$.

**Ans.** (a) –1.70 V; (b) –1.79 V; (c) –0.24 V/V; (d) –0.58 V

**Manufacturers' Specifications** ECL manufacturers supply gate transfer characteristics of the form shown in Figs. 15.29 and 15.31. A manufacturer usually provides such curves measured at a number of temperatures. In addition, at each relevant temperature, worst-case values for the parameters $V_{IL}$, $V_{IH}$, $V_{OL}$, and $V_{OH}$ are given. These worst-case values are specified with the inevitable component tolerances taken into account. As an example, Motorola specifies that for MECL 10,000 at 25°C, the following worst-case

values apply[6]

$$V_{IL\max} = -1.475 \text{ V} \qquad V_{IH\min} = -1.105 \text{ V}$$
$$V_{OL\max} = -1.630 \text{ V} \qquad V_{OH\min} = -0.980 \text{ V}$$

These values can be used to determine worst-case noise margins,

$$NM_L = 0.155 \text{ V} \qquad NM_H = 0.125 \text{ V}$$

which are about half the *typical* values previously calculated.

For additional information on MECL specifications the interested reader is referred to the Motorola (1988, 1989) publications listed in the bibliography in Appendix I.

### 15.4.5 Fan-Out

When the input signal to an ECL gate is low ($V_{OL}$), the input current is equal to the current that flows in the 50-kΩ pull-down resistor. Thus,

$$I_{IL} = \frac{-1.77 + 5.2}{50} \simeq 69\,\mu\text{A}$$

When the input is high ($V_{OH}$), the input current is greater because of the base current of the input transistor. Thus, assuming a transistor $\beta$ of 100, we obtain

$$I_{IH} = \frac{-0.88 + 5.2}{50} + \frac{4}{101} \simeq 126\,\mu\text{A}$$

Both these current values are quite small, which, coupled with the very small output resistance of the ECL gate, ensures that little degradation of logic-signal levels results from the input currents of fan-out gates. It follows that the fan-out of ECL gates is not limited by logic-level considerations but rather by the degradation of the circuit speed (rise and fall times). This latter effect is due to the capacitance that each fan-out gate presents to the driving gate (approximately 3 pF). Thus while the *dc fan-out* can be as high as 90 and thus does not represent a design problem, the *ac fan-out* is limited by considerations of circuit speed to 10 or so.

### 15.4.6 Speed of Operation and Signal Transmission

The speed of operation of a logic family is measured by the delay of its basic gate and by the rise and fall times of the output waveforms. Typical values of these parameters for ECL have already been given. Here we should note that because the output circuit is an emitter follower, the rise time of the output signal is shorter than its fall time, since on the rising edge of the output pulse, the emitter follower functions and provides the output current required to charge up the load and parasitic capacitances. On the other hand, as the signal at the base of the emitter follower falls, the emitter follower cuts off, and the load capacitance discharges through the combination of load and pull-down resistances.

To take full advantage of the very high speed of operation possible with ECL, special attention should be paid to the method of interconnecting the various logic gates in a system. To appreciate this point, we shall briefly discuss the problem of signal transmission.

ECL deals with signals whose rise times may be 1 ns or even less, the time it takes for light to travel only 30 cm or so. For such signals, a wire and its environment become a relatively complex circuit element along which signals propagate with finite speed (perhaps half the speed of light—i.e., 15 cm/ns). Unless special care is taken, energy that reaches the end

[6] MECL is the trade name used by Motorola (now Freescale Semiconductors) for its ECL.

of such a wire is not absorbed but rather returns as a *reflection* to the transmitting end, where (without special care) it may be re-reflected. The result of this process of reflection is what can be observed as **ringing**, a damped oscillatory excursion of the signal about its final value.

Unfortunately, ECL is particularly sensitive to ringing because the signal levels are so small. Thus it is important that transmission of signals be well controlled, and surplus energy absorbed, to prevent reflections. The accepted technique is to limit the nature of connecting wires in some way. One way is to insist that they be very short, where "short" is taken to mean with respect to the signal rise time. The reason for this is that if the wire connection is so short that reflections return while the input is still rising, the result becomes only a somewhat slowed and "bumpy" rising edge.

If, however, the reflection returns *after* the rising edge, it produces not simply a modification of the initiating edge but an *independent second event.* This is clearly bad! Thus the time taken for a signal to go from one end of a line and back is restricted to less than the rise time of the driving signal by some factor—say, 5. Thus for a signal with a 1-ns rise time and for propagation at the speed of light (30 cm/ns), a double path of only 0.2-ns equivalent length, or 6 cm, would be allowed, representing in the limit a wire only 3 cm from end to end.

Such is the restriction on ECL 100K. However, ECL 10K has an intentionally slower rise time of about 3.5 ns. Using the same rules, wires can accordingly be as long as about 10 cm for ECL 10K.

If greater lengths are needed, then transmission lines must be used. These are simply wires in a controlled environment in which the distance to a ground reference plane or a second wire is highly controlled. Thus they might simply be twisted pairs of wires, one of which is grounded, or parallel ribbon wires, every second of which is grounded, or so-called microstrip lines on a printed-circuit board. The latter are simply copper strips of controlled geometry on one side of a thin printed-circuit board, the other side of which consists of a grounded plane.

Such transmission lines have a *characteristic impedance*, $R_0$, that ranges from a few tens of ohms to hundreds of ohms. Signals propagate on such lines somewhat more slowly than the speed of light, perhaps half as fast. When a transmission line is terminated at its receiving end in a resistance equal to its characteristic impedance, $R_0$, all the energy sent on the line is absorbed at the receiving end, and no reflections occur (since the termination acts as a limitless length of transmission line). Thus, signal integrity is maintained. Such transmission lines are said to be *properly terminated.* A properly terminated line appears at its sending end as a resistor of value $R_0$. The followers of ECL 10K with their open emitters and low output resistances (specified to be 7 Ω maximum) are ideally suited for driving transmission lines. ECL is also good as a line receiver. The simple gate with its high (50-kΩ) pull-down input resistor represents a very high resistance to the line. Thus a few such gates can be connected to a terminated line with little difficulty. Both these ideas are represented in Fig. 15.27.

### 15.4.7 Power Dissipation

Because of the differential-amplifier nature of ECL, the gate current remains approximately constant and is simply steered from one side of the gate to the other depending on the input logic signals. Thus, the supply current and hence the gate power dissipation of unterminated ECL remain relatively constant independent of the logic state of the gate. It follows that no voltage spikes are introduced on the supply line. Such spikes can be a dangerous source of noise in a digital system. It follows that in ECL the need for supply-line bypassing[7] is not as great as in, say, TTL. This is another advantage of ECL.

[7] Achieved by connecting capacitances to ground at frequent intervals along the power-supply line on a printed-circuit board.

At this juncture we should reiterate a point we made earlier, namely, that although an ECL gate would operate with $V_{EE} = 0$ and $V_{CC} = +5.2$ V, the selection of $V_{EE} = -5.2$ V and $V_{CC} = 0$ V is recommended, because in the circuit, all signal levels are referenced to $V_{CC}$, and ground is certainly an excellent reference.

**EXERCISE**

**15.16** For the ECL gate in Fig. 15.26, calculate an approximate value for the power dissipated in the circuit under the condition that all inputs are low and that the emitters of the output followers are left open. Assume that the reference circuit supplies four identical gates, and hence only a quarter of the power dissipated in the reference circuit should be attributed to a single gate.
**Ans.** 22.4 mW

### 15.4.8 Thermal Effects

In our analysis of the ECL gate of Fig. 15.26, we found that at room temperature the reference voltage $V_R$ is –1.32 V. We have also shown that the midpoint of the output logic swing is approximately equal to this voltage, which is an ideal situation in that it results in equal high and low noise margins. In Example 15.4, we shall derive expressions for the temperature coefficients of the reference voltage and of the output low and high voltages. In this way, it will be shown that the midpoint of the output logic swing varies with temperature at the same rate as the reference voltage. As a result, although the magnitudes of the high and low noise margins change with temperature, their values remain equal. This is an added advantage of ECL and provides a demonstration of the high degree of design optimization of this gate circuit.

**Example 15.4**

We wish to determine the temperature coefficient of the reference voltage $V_R$ and of the midpoint between $V_{OL}$ and $V_{OH}$.

#### Solution

To determine the temperature coefficient of $V_R$, consider the circuit in Fig. E15.12 and assume that the temperature changes by +1°C. Denoting the temperature coefficient of the diode and transistor voltage drops by $\delta$, where $\delta \simeq -2$ mV/°C, we obtain the equivalent circuit shown in Fig. 15.33. In the latter circuit, the changes in device voltage drops are considered as signals, and hence the power supply is shown as a signal ground.

In the circuit of Fig. 15.33 we have two signal generators, and we wish to analyze the circuit to determine $\Delta V_R$, the change in $V_R$. We shall do so using the principle of superposition.[8] Consider first the branch $R_1$, $D_1$, $D_2$, $2\delta$, and $R_2$, and neglect the signal base current of $Q_1$. The voltage signal at the base of $Q_1$ can be easily obtained from

[8] Although the circuit contains diodes and a transistor, which are nonlinear elements, we can use superposition because we are dealing with small changes in voltages and currents, and thus the diodes and the transistor are replaced by their linear small-signal models.

## Example 15.4 *continued*

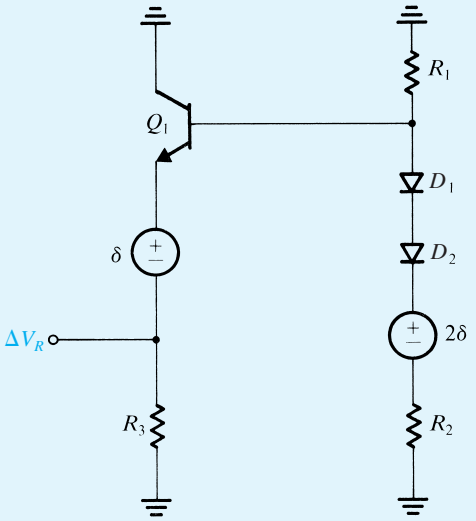


**Figure 15.33** Equivalent circuit for determining the temperature coefficient of the reference voltage $V_R$.

$$v_{b1} = \frac{2\delta \times R_1}{R_1 + r_{d1} + r_{d2} + R_2}$$

where $r_{d1}$ and $r_{d2}$ denote the incremental resistances of diodes $D_1$ and $D_2$, respectively. The dc bias current through $D_1$ and $D_2$ is approximately 0.64 mA, and thus $r_{d1} = r_{d2} = 39.5\,\Omega$. Hence $v_{b1} \simeq 0.3\delta$. Since the gain of the emitter follower $Q_1$ is approximately unity, it follows that the component of $\Delta V_R$ due to the generator $2\delta$ is approximately equal to $v_{b1}$, that is, $\Delta V_{R1} = 0.3\delta$.

Consider next the component of $\Delta V_R$ due to the generator $\delta$. Reflection into the emitter circuit of the total resistance of the base circuit, $\left[R_1 \parallel \left(r_{d1} + r_{d2} + R_2\right)\right]$, by dividing it by $\beta + 1$ (with $\beta \simeq 100$) results in the following component of $\Delta V_R$:

$$\Delta V_{R2} = -\frac{\delta \times R_3}{[R_B/(\beta+1)] + r_{e1} + R_3}$$

Here $R_B$ denotes the total resistance in the base circuit, and $r_{e1}$ denotes the emitter resistance of $Q_1$ ($\simeq 40\,\Omega$). This calculation yields $\Delta V_{R2} \simeq -\delta$. Adding this value to that due to the generator $2\delta$ gives $\Delta V_R \simeq -0.7\delta$. Thus for $\delta = -2$ mV/°C the temperature coefficient of $V_R$ is +1.4 mV/°C.

We next consider the determination of the temperature coefficient of $V_{OL}$. The circuit on which to perform this analysis is shown in Fig. 15.34. Here we have three generators whose contributions can be considered separately and the resulting components of $\Delta V_{OL}$ summed. The result is

$$\begin{aligned}\Delta V_{OL} = {} & \Delta V_R \frac{-R_{C2}}{r_{eR} + R_E} \frac{R_T}{R_T + r_{e2}} \\ & - \delta \frac{-R_{C2}}{r_{eR} + R_E} \frac{R_T}{R_T + r_{e2}} \\ & - \delta \frac{R_T}{R_T + r_{e2} + R_{C2}/(\beta+1)}\end{aligned}$$

**Example 15.4** *continued*

Substituting the values given and those obtained throughout the analysis of this section, we find

$$\Delta V_{OL} \simeq -0.43\delta$$

The circuit for determining the temperature coefficient of $V_{OH}$ is shown in Fig. 15.35, from which we obtain

$$\Delta V_{OH} = -\delta \frac{R_T}{R_T + r_{e2} + R_{C2}/(\beta + 1)} = -0.93\delta$$

We now can obtain the variation of the midpoint of the logic swing as

$$\frac{\Delta V_{OL} + \Delta V_{OH}}{2} = -0.68\delta$$

which is approximately equal to that of the reference voltage $V_R(-0.7\delta)$.

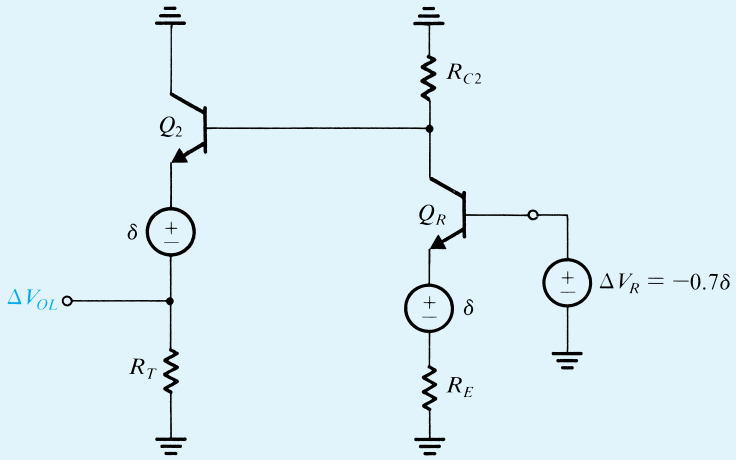


**Figure 15.34** Equivalent circuit for determining the temperature coefficient of $V_{OL}$.

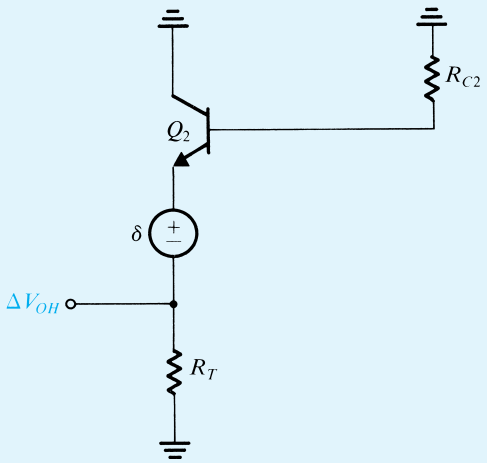


**Figure 15.35** Equivalent circuit for determining the temperature coefficient of $V_{OH}$.

### 15.4.9 The Wired-OR Capability

The emitter–follower output stage of the ECL family allows an additional level of logic to be performed at very low cost by simply wiring the outputs of several gates in parallel. This is illustrated in Fig. 15.36, where the outputs of two gates are wired together. Note that the base–emitter diodes of the output followers realize an OR function: This **wired-OR** connection can be used to provide gates with high fan-in as well as to increase the flexibility of ECL in logic design.

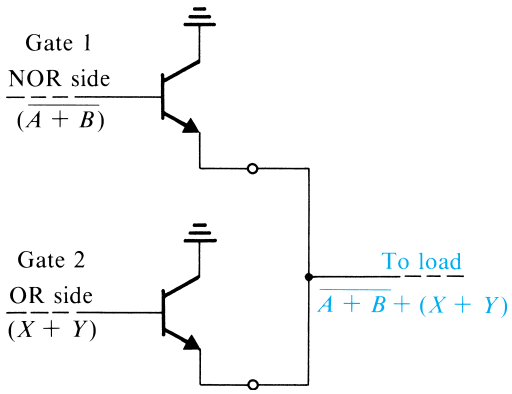


**Figure 15.36** The wired-OR capability of ECL.

### 15.4.10 Final Remarks

We have chosen to study ECL by focusing on a commercially available circuit family. As has been demonstrated, a great deal of design optimization has been applied to create a very-high-performance family of SSI and MSI logic circuits. As already mentioned, ECL and some of its variants are also used in VLSI circuit design. Applications include very-high-speed processors such as those used in supercomputers, as well as high-speed and high-frequency communication systems. When employed in VLSI design, current–source biasing is almost always utilized. Further, a variety of circuit configurations are employed (see Rabaey, 1996).

## 15.5 BiCMOS Digital Circuits

In this section, we provide an introduction to a VLSI circuit technology that is becoming increasingly popular, BiCMOS. As its name implies, BiCMOS technology combines *bi*polar and *CMOS* circuits on one IC chip. The aim is to combine the low-power, high-input impedance and wide noise margins of CMOS with the high current-driving capability of bipolar transistors. Specifically, CMOS, although a nearly ideal logic-circuit technology in many respects, has a limited current-driving capability. This is not a serious problem when the CMOS gate has to drive a few other CMOS gates. It becomes a serious issue, however, when relatively large capacitive loads (e.g., greater than 0.5 pF or so) are present. In such cases, one has to either resort to the use of elaborate CMOS buffer circuits or face the usually unacceptable consequence of long propagation delays. On the other hand, we know that by virtue of its much larger transconductance, the BJT is capable of large output currents. We have seen a practical illustration of that in the emitter–follower output stage of ECL.

Indeed, the high current-driving capability contributes to making ECL two to five times faster than CMOS (under equivalent conditions)—of course, at the expense of high power dissipation. In summary, then, BiCMOS seeks to combine the best of the CMOS and bipolar technologies to obtain a class of circuits that is particularly useful when output currents that are higher than possible with CMOS are needed. Furthermore, since BiCMOS technology is well suited for the implementation of high-performance analog circuits (see, e.g., Section 8.3), it makes possible the realization of both analog and digital functions on the same IC chip, making the "**system on a chip**" an attainable goal. The price paid is a more complex, and hence more expensive (than CMOS) processing technology.

### 15.5.1 The BiCMOS Inverter

A variety of BiCMOS inverter circuits have been proposed and are in use. All of these are based on the use of *npn* transistors to increase the output current available from a CMOS inverter. This can be most simply achieved by cascading each of the $Q_N$ and $Q_P$ devices of the CMOS inverter with an *npn* transistor, as shown in Fig. 15.37(a). Observe that this circuit can be thought of as utilizing the pair of complementary composite MOS-BJT devices shown in Fig. 15.37(b). These composite devices[9] retain the high input impedance of the MOS transistor while in effect multiplying its rather low $g_m$ by the $\beta$ of the BJT. It is also useful to observe that the output stage formed by $Q_1$ and $Q_2$ has what is known as the **totem-pole configuration** utilized by TTL.[10]

The circuit of Fig. 15.37(a) operates as follows: When $v_I$ is low, both $Q_N$ and $Q_2$ are off while $Q_P$ conducts and supplies $Q_1$ with base current, thus turning it on. Transistor $Q_1$ then provides a large output current to charge the load capacitance. The result is a very fast charging of the load capacitance and correspondingly a short low-to-high propagation delay, $t_{PLH}$. Transistor $Q_1$ turns off when $v_O$ reaches a value of about $V_{DD} - V_{BE1}$, and thus the output high level is lower than $V_{DD}$, a disadvantage. When $v_I$ goes high, $Q_P$ and $Q_1$ turn off, and $Q_N$ turns on, providing its drain current into the base of $Q_2$. Transistor $Q_2$ then turns on and provides a large output current that quickly discharges the load capacitance. Here again the result is a short high-to-low propagation delay, $t_{PHL}$. On the negative side, $Q_2$ turns off when $v_O$ reaches a value of about $V_{BE2}$, and thus the output low level is greater than zero, a disadvantage.

Thus, while the circuit of Fig. 15.37(a) features large output currents and short propagation delays, it has the disadvantage of reduced logic swing and, correspondingly, reduced noise margins. There is also another and perhaps more serious disadvantage, namely, the relatively long turn-off delays of $Q_1$ and $Q_2$ arising from the absence of circuit paths along which the base charge can be removed. This problem can be solved by adding a resistor between the base of each of $Q_1$ and $Q_2$ and ground, as shown in Fig. 15.37(c). Now when either $Q_1$ or $Q_2$ is turned off, its stored base charge is removed to ground through $R_1$ or $R_2$, respectively. Resistor $R_2$ provides an additional benefit: With $v_I$ high, and after $Q_2$ cuts off, $v_O$ continues to fall below $V_{BE2}$, and the output node is pulled to ground through the series path of $Q_N$ and $R_2$. Thus $R_2$ functions as a pull-down resistor. The $Q_N$–$R_2$ path, however, is a high-impedance one with the result that pulling $v_O$ to ground is a rather slow process. Incorporating the resistor $R_1$, however, is disadvantageous from a static power-dissipation standpoint: When $v_I$ is low, a dc path exists between $V_{DD}$ and ground through the conducting $Q_P$ and $R_1$. Finally, it should

[9] It is interesting to note that these composite devices were proposed as early as 1969 (see Lin et al., 1969).

[10] Refer to the book's website for a description of the basic TTL logic-gate circuit and its totem-pole output stage.

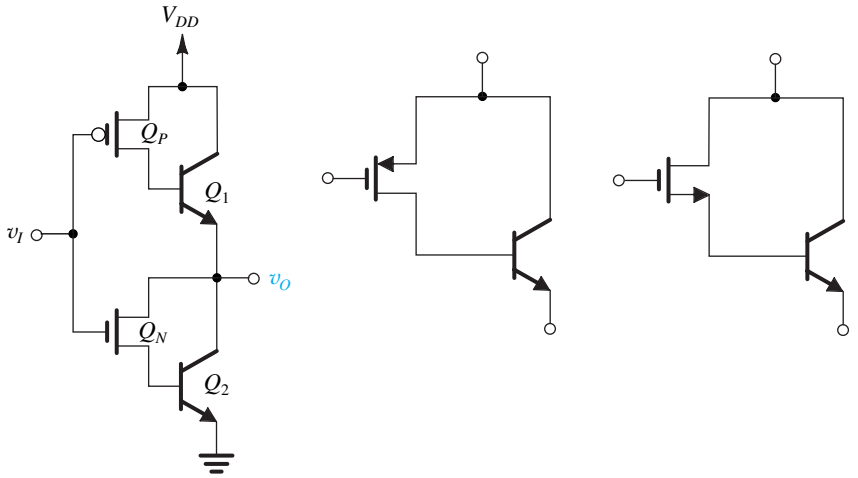


**Figure 15.37** Development of the BiCMOS inverter circuit. **(a)** The basic concept is to use an additional bipolar transistor to increase the output current drive of each of $Q_N$ and $Q_P$ of the CMOS inverter. **(b)** The circuit in **(a)** can be thought of as utilizing these composite devices. **(c)** To reduce the turn-off times of $Q_1$ and $Q_2$, "bleeder resistors" $R_1$ and $R_2$ are added. **(d)** Implementation of the circuit in **(c)** using NMOS transistors to realize the resistors. **(e)** An improved version of the circuit in **(c)** obtained by connecting the lower end of $R_1$ to the output node.

be noted that $R_1$ and $R_2$ take some of the drain currents of $Q_P$ and $Q_N$ away from the bases of $Q_1$ and $Q_2$ and thus slightly reduce the gate output current available to charge and discharge the load capacitance.

Figure 15.37(d) shows the way in which $R_1$ and $R_2$ are usually implemented. As indicated, NMOS devices $Q_{R1}$ and $Q_{R2}$ are used to realize $R_1$ and $R_2$. As an added innovation, these two transistors are made to conduct only when needed. Thus, $Q_{R1}$ will conduct only when $v_I$ rises, at which time its drain current constitutes a reverse base current for $Q_1$, speeding up its turn-off. Similarly, $Q_{R2}$ will conduct only when $v_I$ falls and $Q_P$ conducts, pulling the gate of $Q_{R2}$ high. The drain current of $Q_{R2}$ then constitutes a reverse base current for $Q_2$, speeding up its turn-off.

As a final circuit for the BiCMOS inverter, we show the so-called *R*-circuit in Fig. 15.37(e). This circuit differs from that in Fig. 15.37(c) in only one respect: Rather than returning $R_1$ to ground, we have connected $R_1$ to the output node of the inverter. This simple change has two benefits. First, the problem of static power dissipation is now solved. Second, $R_1$ now functions as a pull-up resistor, pulling the output node voltage up to $V_{DD}$ (through the conducting $Q_P$) after $Q_1$ has turned off. Thus, the *R* circuit in Fig. 15.37(e) does in fact have output levels very close to $V_{DD}$ and ground.

As a final remark on the BiCMOS inverter, we note that the circuit is designed so that transistors $Q_1$ and $Q_2$ are never simultaneously conducting and neither is allowed to saturate. Unfortunately, sometimes the resistance of the collector region of the BJT in conjunction with large capacitive-charging currents causes saturation to occur. Specifically, at large output currents, the voltage developed across $r_C$ (which can be of the order of 100 Ω) can lower the voltage at the intrinsic collector terminal and cause the CBJ to become forward biased. As the reader will recall, saturation is a harmful effect for two reasons: It limits the collector current to a value less than $\beta I_B$, and it slows down the transistor turn-off.

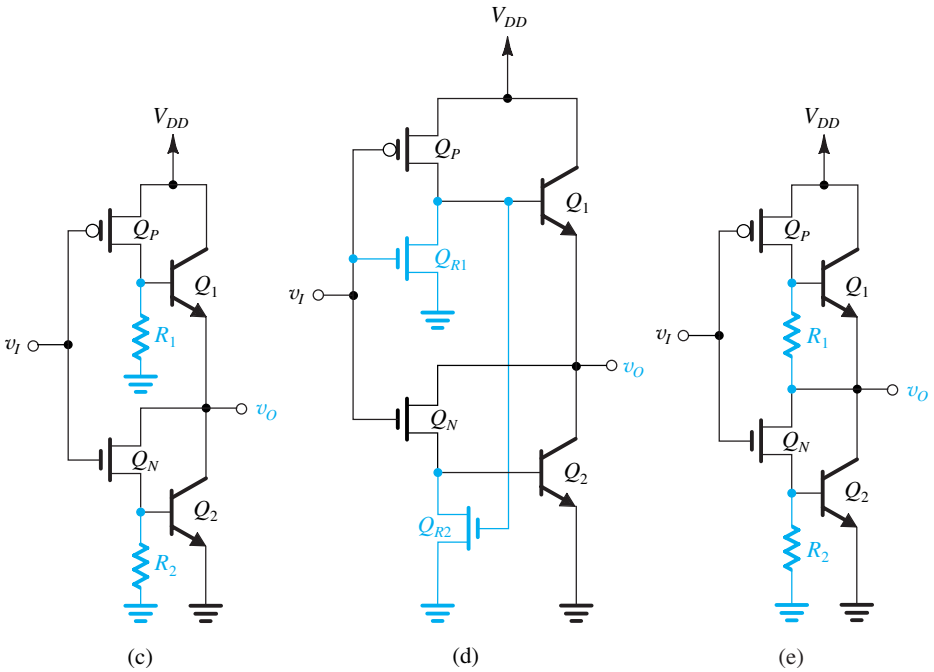


**Figure 15.37** *continued*

## 15.5.2 Dynamic Operation

A detailed analysis of the dynamic operation of the BiCMOS inverter circuit is a rather complex undertaking. Nevertheless, an estimate of its propagation delay can be obtained by considering only the time required to charge and discharge a load capacitance $C$. Such an approximation is justified when $C$ is relatively large and thus its effect on inverter dynamics is dominant: in other words, when we are able to neglect the time required to charge the parasitic capacitances present at internal circuit nodes. Fortunately, this is usually the case in practice, for if the load capacitance is not large, one would use the simpler CMOS inverter. In fact, it has been shown (Embabi, Bellaouar, and Elmasry, 1993) that the speed advantage of Bi-CMOS (over CMOS) becomes evident only when the gate is required to drive a large fan-out or a large load capacitance. For instance, at a load capacitance of 50 fF to 100 fF, BiCMOS and CMOS typically feature equal delays. However, at a load capacitance of 1 pF, $t_P$ of a BiCMOS inverter is 0.3 ns, whereas that of an otherwise comparable CMOS inverter is about 1 ns.

Finally, in Fig. 15.38, we show simplified equivalent circuits that can be employed in obtaining rough estimates of $t_{PLH}$ and $t_{PHL}$ of the $R$-type BiCMOS inverter (see Problem 15.49).

## 15.5.3 BiCMOS Logic Gates

In BiCMOS, the logic is performed by the CMOS part of the gate, with the bipolar portion simply functioning as an output stage. It follows that BiCMOS logic-gate circuits can be generated following the same approach used in CMOS. As an example, we show in Fig. 15.39 a BiCMOS two-input NAND gate.

As a final remark, we note that BiCMOS technology is applied in a variety of products including microprocessors, static RAMs, and gate arrays (see Alvarez, 1993).

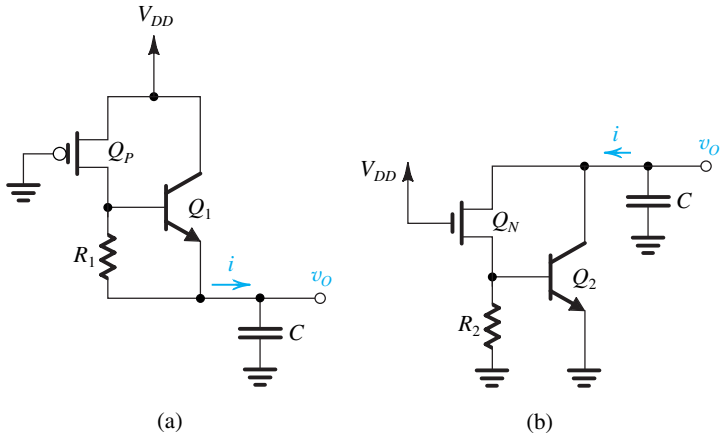


**Figure 15.38** Equivalent circuits for charging and discharging a load capacitance $C$. Note that $C$ includes all the capacitances present at the output node.

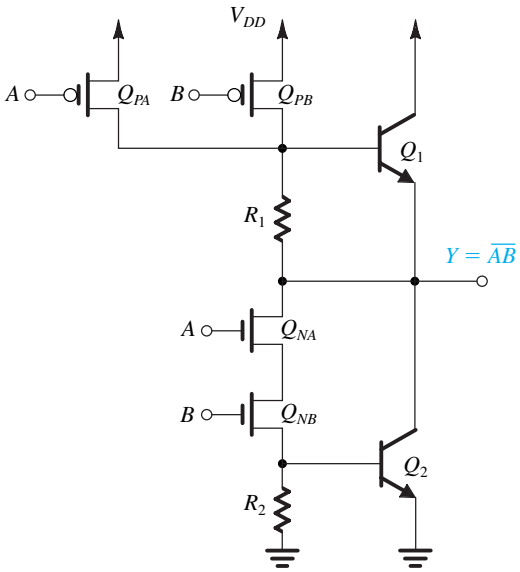


**Figure 15.39** A BiCMOS two-input NAND gate.

## EXERCISE

**D15.17** The threshold voltage of the BiCMOS inverter of Fig. 15.37(e) is the value of $v_I$ at which both $Q_N$ and $Q_P$ are conducting equal currents and operating in the saturation region. At this value of $v_I$, $Q_2$ will be on, causing the voltage at the source of $Q_N$ to be approximately 0.7 V. It is required to design the circuit so that the threshold voltage is equal to $V_{DD}/2$. For $V_{DD} = 5$ V, $|V_t| = 0.6$ V, and assuming equal channel lengths for $Q_N$ and $Q_P$ and that $\mu_n \simeq 2.5\,\mu_p$, find the required ratio of widths, $W_p/W_n$.
**Ans.** 1

## Section 15.4: Emitter-Coupled Logic (ECL)

**D 15.34** For the ECL circuit in Fig. P15.34, the transistors exhibit $V_{BE}$ of 0.75 V at an emitter current $I$ and have very high $\beta$.

(a) Find $V_{OH}$ and $V_{OL}$.
(b) For the input at $B$ that is sufficiently negative for $Q_B$ to be cut off, what voltage at $A$ causes a current of $I/2$ to flow in $Q_R$?
(c) Repeat (b) for a current in $Q_R$ of $0.99I$.
(d) Repeat (c) for a current in $Q_R$ of $0.01I$.
(e) Use the results of (c) and (d) to specify $V_{IL}$ and $V_{IH}$.
(f) Find $NM_H$ and $NM_L$.
(g) Find the value of $IR$ that makes the noise margins equal to the width of the transition region, $V_{IH}-V_{IL}$.
(h) Using the $IR$ value obtained in (g), give numerical values for $V_{OH}$, $V_{OL}$, $V_{IH}$, $V_{IL}$, and $V_R$ for this ECL gate.

***15.35** Three logic inverters are connected in a ring. Specifications for this family of gates indicate a typical propagation delay of 3 ns for high-to-low output transitions and 7 ns for low-to-high transitions. Assume that for some reason the input to one of the gates undergoes a low-to-high transition. By sketching the waveforms at the outputs of the three gates and keeping track of their relative positions, show that the circuit functions as an oscillator. What is the frequency of oscillation of this ring oscillator? In each cycle, how long is the output high? low?

***15.36** Following the idea of a ring oscillator introduced in Problem 15.35, consider an implementation using a ring of five ECL 100K inverters. Assume that the inverters have linearly rising and falling edges (and thus the waveforms are trapezoidal in shape). Let the 0 to 100% rise and fall times be equal to 1 ns. Also, let the propagation delay (for both transitions) be equal to 1 ns. Provide a labeled sketch of the five output signals, taking care that relevant phase information is provided. What is the frequency of oscillation?

**D *15.37** Using the logic and circuit flexibility of ECL indicated by Figs. 15.26 and 15.36, sketch an ECL logic circuit that realizes the exclusive OR function, $Y = \overline{A}B + A\overline{B}$. Give a logic diagram (as opposed to a circuit diagram).

***15.38** For the circuit in Fig. 15.28 whose transfer characteristic is shown in Fig. 15.29, calculate the incremental voltage gain from input to the OR output at points $x$, $m$, and $y$ of the transfer characteristic. Assume $\beta = 100$. Use the results of Exercise 15.14, and let the output at $x$ be –1.77 V and that at $y$ be –0.88 V. (*Hint*: Recall that $x$ and $y$ are defined by a 1%, 99% current split.)

**15.39** For the circuit in Fig. 15.28 whose transfer characteristic is shown in Fig. 15.29, find $V_{IL}$ and $V_{IH}$ if $x$ and $y$ are defined as the points at which

(a) 90% of the current $I_E$ is switched.
(b) 99.9% of the current $I_E$ is switched.

**15.40** For the symmetrically loaded circuit of Fig. 15.28 and for typical output signal levels ($V_{OH} = -0.88$ V and

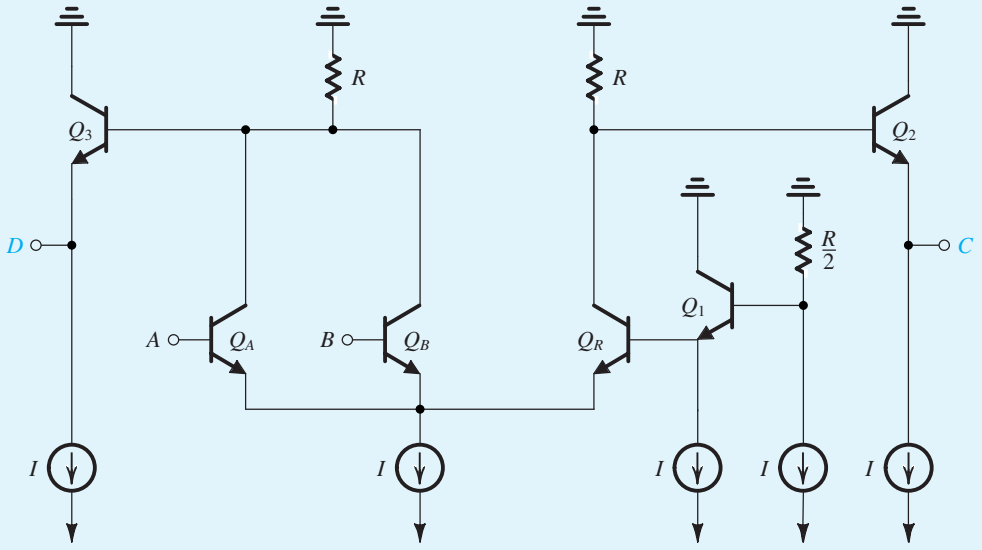


Figure P15.34

$V_{OL} = -1.77$ V), calculate the power lost in both load resistors $R_T$ and both output followers. What then is the total power dissipation of a single ECL gate, including its symmetrical output terminations?

**15.41** Considering the circuit of Fig. 15.30, what is the value of $\beta$ of $Q_2$, for which the high noise margin ($NM_H$) is reduced by 50%?

***15.42** Consider an ECL gate whose inverting output is terminated in a 50-Ω resistance connected to a –2-V supply. Let the total load capacitance be denoted $C$. As the input of the gate rises, the output emitter follower cuts off and the load capacitance $C$ discharges through the 50-Ω load (until the emitter follower conducts again). Find the value of $C$ that will result in a discharge time of 1 ns. Assume that the two output levels are –0.88 V and –1.77 V.

**15.43** For signals whose rise and fall times are 3.5 ns, what length of unterminated gate-to-gate wire interconnect can be used if a ratio of rise time to return time of 5 to 1 is required? Assume the environment of the wire to be such that the signal propagates at two-thirds the speed of light (which is 30 cm/ns).

***15.44** For the circuit in Fig. P15.44, let the levels of the inputs $A$, $B$, $C$, and $D$ be 0 and +5 V. For all inputs low at 0 V, what is the voltage at $E$? If $A$ and $C$ are raised to +5 V, what is the voltage at $E$? Assume $|V_{BE}| = 0.7$ V and $\beta = 50$. Express $E$ as a logic function of $A$, $B$, $C$, and $D$.

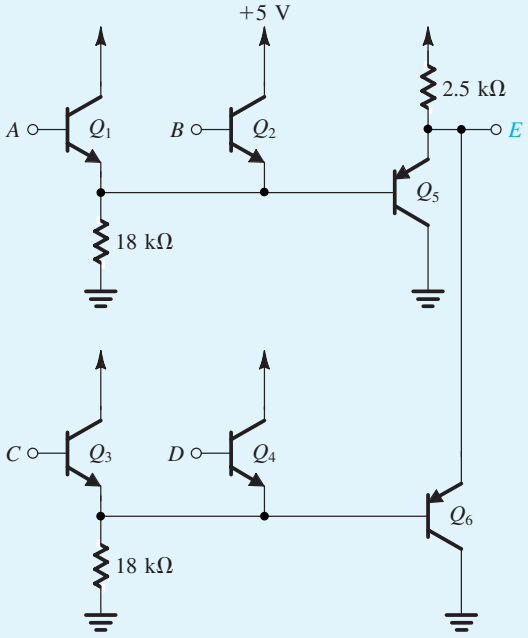


Figure P15.44

## Section 15.5: BiCMOS Digital Circuits

**15.45** Consider the conceptual BiCMOS circuit of Fig. 15.37(a), for the conditions that $V_{DD} = 5$ V, $|V_t| = 1$ V, $V_{BE} = 0.7$ V, $\beta = 100$, $k_n' = 2.5k_p' = 100\,\mu\text{A/V}^2$, and $(W/L)_n = 2\,\mu\text{m}/1\,\mu\text{m}$. For $v_I = v_O = V_{DD}/2$, find $(W/L)_p$ so that $I_{EQ1} = I_{EQ2}$. What is this totem-pole transient current?

**15.46** Consider the conceptual BiCMOS circuit of Fig. 15.37(a) for the conditions stated in Problem 15.45. What is the threshold voltage of the inverter if both $Q_N$ and $Q_P$ have $W/L = 2\,\mu m/1\,\mu m$? What totem-pole current flows at $v_I$ equal to the threshold voltage?

**D *15.47** Consider the choice of values for $R_1$ and $R_2$ in the circuit of Fig. 15.37(c). An important consideration in making this choice is that the loss of base drive current will be limited. This loss becomes particularly acute when the current through $Q_N$ and $Q_P$ becomes small. This in turn happens near the end of the output signal swing when the associated MOS device is deeply in triode operation (say at $|v_{DS}| = |V_t|/3$). Determine values for $R_1$ and $R_2$ so that the loss in base current is limited to 50%. What is the ratio $R_1/R_2$? Repeat for a 20% loss in base drive.

***15.48** For the circuit of Fig. 15.37(a) with parameters as in Problem 15.45 and with $(W/L)_p = (W/L)_n$, estimate the propagation delays $t_{PLH}$, $t_{PHL}$ and $t_P$ obtained for a load capacitance of 2 pF. Assume that the internal node capacitances do not contribute much to this result. Use average values for the charging and discharging currents.

***15.49** Repeat Problem 15.48 for the circuit in Fig. 15.37(e), assuming that $R_1 = R_2 = 5$ kΩ.

**D 15.50** Consider the dynamic response of the NAND gate of Fig. 15.39 with a large external capacitive load. If the worst-case response is to be identical to that of the inverter of Fig. 15.37(e), how must the $W/L$ ratios of $Q_{NA}$, $Q_{NB}$, $Q_N$, $Q_{PA}$, $Q_{PB}$, and $Q_P$ be related?

**D 15.51** Sketch the circuit of a BiCMOS two-input NOR gate. If, when loaded with a large capacitance, the gate is to have worst-case delays equal to the corresponding values of the inverter of Fig. 15.37(e), find $W/L$ of each transistor in terms of $(W/L)_n$ and $(W/L)_p$.

## 18.9 Precision Rectifier Circuits

Rectifier circuits were studied in Chapter 4, where the emphasis was on their application in power-supply design. In such applications, the voltages being rectified are usually much greater than the diode voltage drop, rendering the exact value of the diode drop unimportant to the proper operation of the rectifier. Other applications exist, however, where this is not the case. For instance, in instrumentation applications, the signal to be rectified can be of a very small amplitude, say 0.1 V, making it impossible to employ the conventional rectifier circuits. Also, in instrumentation applications, the need arises for rectifier circuits with very precise transfer characteristics.

Here we study circuits that combine diodes and op amps to implement a variety of rectifier circuits with precise characteristics. Precision rectifiers, which can be considered a special class of wave-shaping circuits, find application in the design of instrumentation systems. An introduction to precision rectifiers was presented in Section 4.5.5. This material, however, is repeated here for the reader's convenience.

### 18.9.1 Precision Half-Wave Rectifier: The "Superdiode"

Figure 18.35(a) shows a precision half-wave-rectifier circuit consisting of a diode placed in the negative-feedback path of an op amp, with $R$ being the rectifier load resistance. The circuit works as follows: If $v_I$ goes positive, the output voltage $v_A$ of the op amp will go positive and the diode will conduct, thus establishing a closed feedback path between the op amp's output terminal and the negative input terminal. This negative-feedback path will cause a virtual short circuit to appear between the two input terminals of the op amp. Thus the voltage at the negative input terminal, which is also the output voltage $v_O$, will equal (to within a few millivolts) that at the positive input terminal, which is the input voltage $v_I$,

$$v_O = v_I \quad v_I \geq 0$$

Note that the offset voltage ($\simeq 0.5$ V) exhibited in the simple half-wave-rectifier circuit is no longer present. For the op-amp circuit to start operation, $v_I$ has to exceed only a negligibly small voltage equal to the diode drop divided by the op amp's open-loop gain. In other words, the straight-line transfer characteristic $v_O$–$v_I$ almost passes through the origin. This makes this circuit suitable for applications involving very small signals.

Consider now the case when $v_I$ goes negative. The op amp's output voltage $v_A$ will tend to follow and go negative. This will reverse-bias the diode, and no current will flow through resistance $R$, so that $v_O$ remains equal to 0 V. Thus for $v_I < 0$, $v_O = 0$. Since in this case the diode is off, the op amp will be operating in an open-loop fashion and its output will be at the negative saturation level.

The transfer characteristic of this circuit will be that shown in Fig. 18.35(b), which is almost identical to the ideal characteristic of a half-wave rectifier. The nonideal diode characteristics have been almost completely masked by placing the diode in the negative-feedback path of an op amp. This is another dramatic application of negative feedback. The combination of diode and op amp, shown in the dashed box in Fig. 18.35(a), is appropriately referred to as a "superdiode."

As usual, though, not all is well. The circuit of Fig. 18.35 has some disadvantages: When $v_I$ goes negative and $v_O = 0$, the entire magnitude of $v_I$ appears between the two input terminals of the op amp. If this magnitude is greater than a few volts, the op amp may be damaged unless it is equipped with what is called "overvoltage protection" (a feature that most modern IC

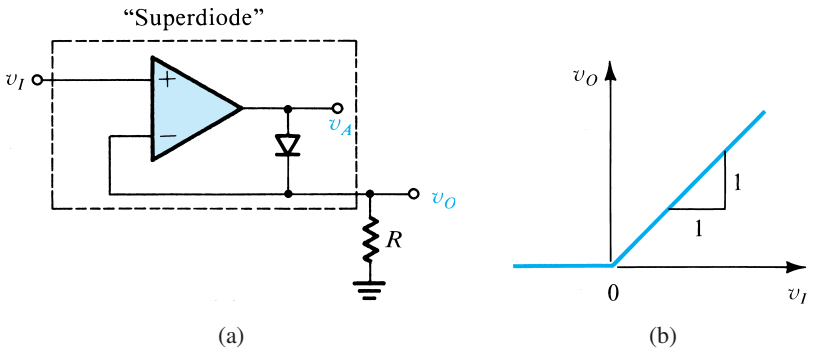


**Figure 18.35** **(a)** The "superdiode" precision half-wave rectifier; **(b)** its almost ideal transfer characteristic. Note that when $v_I > 0$ and the diode conducts, the op amp supplies the load current, and the source is conveniently buffered, an added advantage.

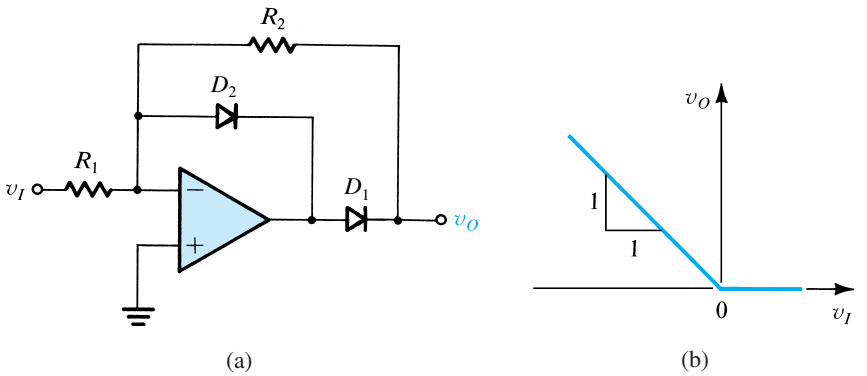


**Figure 18.36** **(a)** An improved version of the precision half-wave rectifier: Diode $D_2$ is included to keep the feedback loop closed around the op amp during the off times of the rectifier diode $D_1$, thus preventing the op amp from saturating. **(b)** The transfer characteristic for $R_2 = R_1$.

op amps have). Another disadvantage is that when $v_I$ is negative, the op amp will be saturated. Although not harmful to the op amp, saturation should usually be avoided, since getting the op amp out of the saturation region and back into its linear region of operation requires some time. This time delay will obviously slow down circuit operation and limit the frequency of operation of the superdiode half-wave-rectifier circuit.

## 18.9.2 An Alternative Circuit

An alternative precision rectifier circuit that does not suffer from the disadvantages mentioned above is shown in Fig. 18.36. The circuit operates in the following manner: For positive $v_I$, diode $D_2$ conducts and closes the negative-feedback loop around the op amp. A virtual ground therefore will appear at the inverting input terminal, and the op amp's output will be *clamped* at one diode drop below ground. This negative voltage will keep diode $D_1$ off, and no current will flow in the feedback resistance $R_2$. It follows that the rectifier output voltage will be zero.

As $v_I$ goes negative, the voltage at the inverting input terminal will tend to go negative, causing the voltage at the op amp's output terminal to go positive. This will cause $D_2$ to be

reverse-biased and hence to be cut off. Diode $D_1$, however, will conduct through $R_2$, thus establishing a negative-feedback path around the op amp and forcing a virtual ground to appear at the inverting input terminal. The current through the feedback resistance $R_2$ will be equal to the current through the input resistance $R_1$. Thus for $R_1 = R_2$ the output voltage $v_O$ will be

$$v_O = -v_I \quad v_I \leq 0$$

The transfer characteristic of the circuit is shown in Fig. 18.36(b). Note that unlike the situation for the circuit shown in Fig. 18.35, here the slope of the characteristic can be set to any desired value, including unity, by selecting appropriate values for $R_1$ and $R_2$.

As mentioned before, the major advantage of the improved half-wave-rectifier circuit is that the feedback loop around the op amp remains closed at all times. Hence the op amp remains in its linear operating region, avoiding the possibility of saturation and the associated time delay required to "get out" of saturation. Diode $D_2$ "catches" the op-amp output voltage as it goes negative and clamps it to one diode drop below ground; hence $D_2$ is called a "catching diode."

## 18.9.3 An Application: Measuring AC Voltages

As one of the many possible applications of the precision rectifier circuits discussed in this section, consider the basic ac voltmeter circuit shown in Fig. 18.37. The circuit consists of a half-wave rectifier—formed by op amp $A_1$, diodes $D_1$ and $D_2$, and resistors $R_1$ and $R_2$—and a first-order low-pass filter—formed by op amp $A_2$, resistors $R_3$ and $R_4$, and capacitor $C$. For an input sinusoid having a peak amplitude $V_p$ the output $v_1$ of the rectifier will consist of a half sine wave having a peak amplitude of $V_pR_2/R_1$. It can be shown using Fourier series analysis that the waveform of $v_1$ has an average value of $(V_p/\pi)(R_2/R_1)$ in addition to

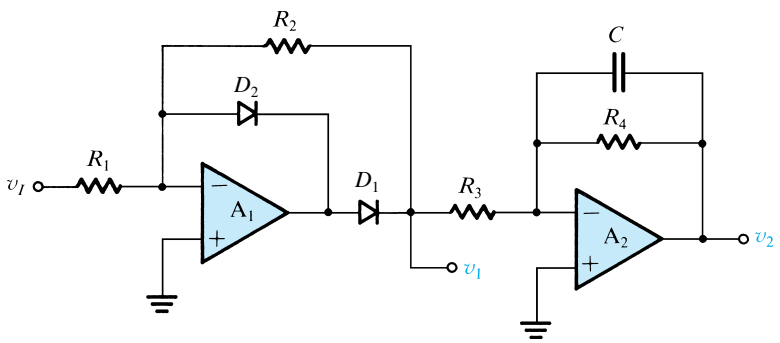


**Figure 18.37** A simple ac voltmeter consisting of a precision half-wave rectifier followed by a first-order low-pass filter.

## EXERCISES

**18.27** Consider the operational rectifier or superdiode circuit of Fig. 18.35(a), with $R = 1\,\text{k}\Omega$. For $v_I = 10\,\text{mV}$, 1 V, and –1 V, what are the voltages that result at the rectifier output and at the output of the op amp?

Assume that the op amp is ideal and that its output saturates at ±12 V. The diode has a 0.7-V drop at 1-mA current, and the voltage drop changes by 0.1 V per decade of current change.

**Ans.** 10 mV, 0.51 V; 1 V, 1.7 V; 0 V, –12 V

**18.28** If the diode in the circuit of Fig. 18.35(a) is reversed, what is the transfer characteristic $v_O$ as a function of $v_I$?

**Ans.** $v_O = 0$ for $v_I \geq 0$; $v_O = v_I$ for $v_I \leq 0$

**18.29** Consider the circuit in Fig. 18.36(a) with $R_1 = 1$ kΩ and $R_2 = 10$ kΩ. Find $v_O$ and the voltage at the amplifier output for $v_I = +1$ V, –10 mV, and –1 V. Assume the op amp to be ideal with saturation voltages of ±12 V. The diodes have 0.7-V voltage drops at 1 mA, and the voltage drop changes by 0.1 V per decade of current change.

**Ans.** 0 V, −0.vm7 V; 0.1 V, 0.6 V; 10 V, 10.7 V

**18.30** If the diodes in the circuit of Fig. 18.36(a) are reversed, what is the transfer characteristic $v_O$ as a function of $v_I$?

**Ans.** $v_O = -(R_2/R_1)v_I$ for $v_I \geq 0$; $v_O = 0$ for $v_I \leq 0$

**18.31** Find the transfer characteristic for the circuit in Fig. E18.31.

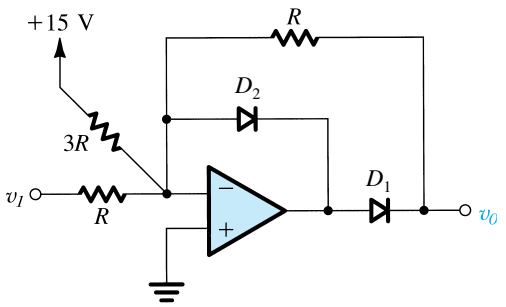


**Figure E18.31**

**Ans.** $v_O = 0$ for $v_I \geq -5$V; $v_O = -v_I - 5$ for $v_I \leq -5$ V

harmonics of the frequency $\omega$ of the input signal. To reduce the amplitudes of all these harmonics to negligible levels, the corner frequency of the low-pass filter should be chosen to be much smaller than the lowest expected frequency $\omega_{\min}$ of the input sine wave. This leads to

$$\frac{1}{CR_4} \ll \omega_{\min}$$

Then the output voltage $v_2$ will be mostly dc, with a value

$$V_2 = -\frac{V_p}{\pi}\frac{R_2}{R_1}\frac{R_4}{R_3}$$

where $R_4/R_3$ is the dc gain of the low-pass filter. Note that this voltmeter essentially measures the average value of the negative parts of the input signal but can be calibrated to provide rms readings for input sinusoids.

### 18.9.4 Precision Full-Wave Rectifier

We now derive a circuit for a precision full-wave rectifier. From Chapter 4 we know that full-wave rectification is achieved by inverting the negative halves of the input-signal waveform and applying the resulting signal to another diode rectifier. The outputs of the two rectifiers are then joined to a common load. Such an arrangement is depicted in Fig. 18.38, which also shows the waveforms at various nodes. Now replacing diode $D_A$ with a superdiode, and replacing diode $D_B$ and the inverting amplifier with the inverting precision half-wave rectifier of Fig. 18.36 but without the catching diode, we obtain the precision full-wave-rectifier circuit of Fig. 18.39(a).

To see how the circuit of Fig. 18.39(a) operates, consider first the case of positive input at A. The output of $A_2$ will go positive, turning $D_2$ on, which will conduct through $R_L$ and thus close the feedback loop around $A_2$. A virtual short circuit will thus be established between the two input terminals of $A_2$, and the voltage at the negative-input terminal, which is the output voltage of the circuit, will become equal to the input. Thus no current will flow through $R_1$ and $R_2$, and the voltage at the inverting input of $A_1$ will be equal to the input and hence positive. Therefore the output terminal (F) of $A_1$ will go negative until $A_1$ saturates. This causes $D_1$ to be turned off.

Next consider what happens when A goes negative. The tendency for a negative voltage at the negative input of $A_1$ causes F to rise, making $D_1$ conduct to supply $R_L$ and allowing the feedback loop around $A_1$ to be closed. Thus a virtual ground appears at the negative input of $A_1$, and the two equal resistances $R_1$ and $R_2$ force the voltage at C, which is the output

## EXERCISES

**18.32** In the full-wave rectifier circuit of Fig. 18.39(a), let $R_1 = R_2 = R_L = 10$ kΩ and assume the op amps to be ideal except for output saturation at ±12 V. When conducting a current of 1 mA, each diode exhibits a voltage drop of 0.7 V, and this voltage changes by 0.1 V per decade of current change. Find $v_O$, $v_E$, and $v_F$ corresponding to $v_I = +0.1$ V, +1 V, +10 V, –0.1 V, and −10 V.
**Ans.** + 0.1 V, + 0.6 V, –12 V; +1 V, +1.6 V, –12 V; +10 V, +10.7 V, –12 V; + 0.1 V, −12 V, + 0.63 V; +1 V, –12 V, +1.63 V; +10 V, –12 V, +10.73 V

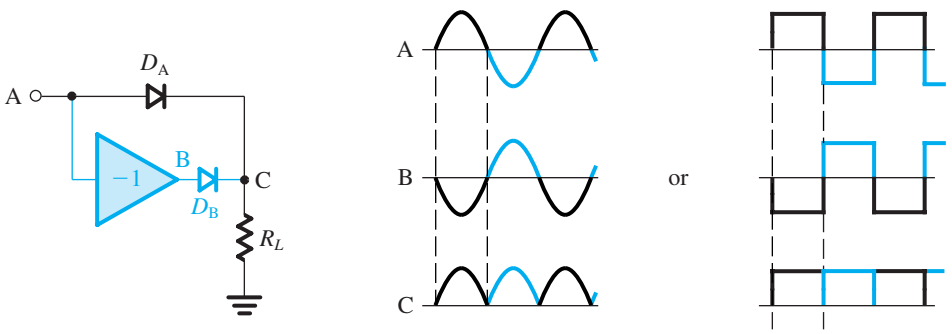


**Figure 18.38** Principle of full-wave rectification.

**D18.33** The block diagram shown in Fig. E18.33(a) gives another possible arrangement for implementing the absolute-value or full-wave-rectifier operation depicted symbolically in Fig. E18.33(b). The block diagram consists of two boxes: a half-wave rectifier, which can be implemented by the circuit in Fig. 18.36(a) after reversing both diodes, and a weighted inverting summer. Convince yourself that this block diagram does in fact realize the absolute-value operation. Then draw a complete circuit diagram, giving reasonable values for all resistors.

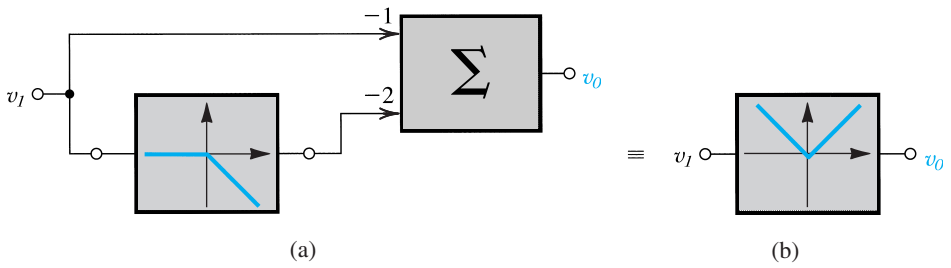


**Figure E18.33**

voltage, to be equal to the negative of the input voltage at A and thus positive. The combination of positive voltage at C and negative voltage at A causes the output of $A_2$ to saturate in the negative direction, thus keeping $D_2$ off.

The overall result is perfect full-wave rectification, as represented by the transfer characteristic in Fig. 18.39(b). This precision is, of course, a result of placing the diodes in op-amp feedback loops, thus masking their nonidealities. This circuit is one of many possible precision full-wave-rectifier or **absolute-value circuits**. Another related implementation of this function is examined in Exercise 18.33.

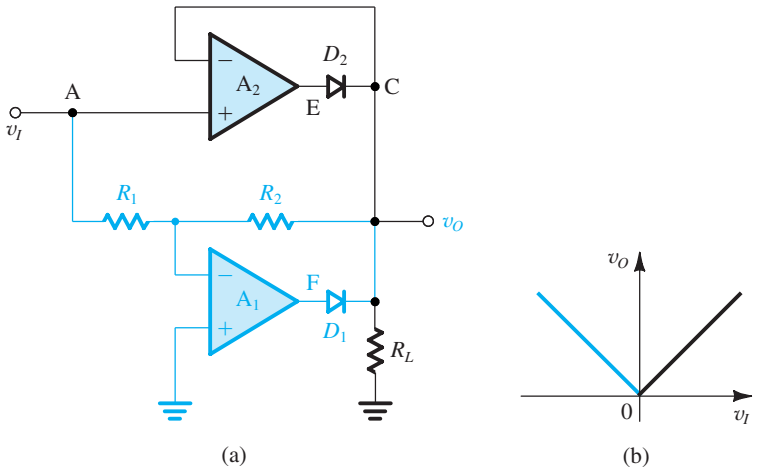


**Figure 18.39** **(a)** Precision full-wave rectifier based on the conceptual circuit of Fig. 18.38. (**b**) Transfer characteristic of the circuit in **(a)**.

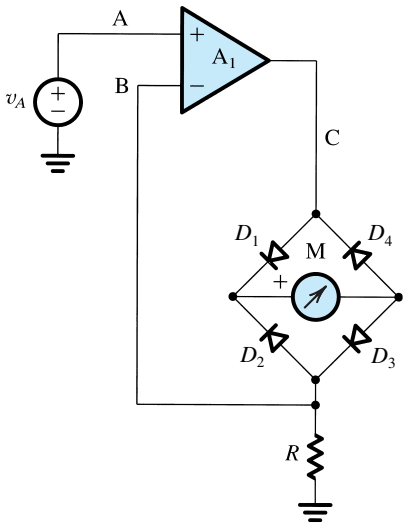


**Figure 18.40** Use of the diode bridge in the design of an ac voltmeter.

## 18.9.5 A Precision Bridge Rectifier for Instrumentation Applications

The bridge rectifier circuit studied in Section 4.5.3 can be combined with an op amp to provide useful precision circuits. One such arrangement is shown in Fig. 18.40. This circuit causes a current equal to $|v_A|/R$ to flow through the moving-coil meter M. Thus the meter provides a reading that is proportional to the average of the absolute value of the input voltage $v_A$. All the nonidealities of the meter and of the diodes are masked by placing the bridge circuit in the negative-feedback loop of the op amp. Observe that when $v_A$ is positive, current flows from the op-amp output through $D_1$, M, $D_3$, and $R$. When $v_A$ is negative, current flows into the op-amp output through $R$, $D_2$, M, and $D_4$. Thus the feedback loop remains closed for both polarities of $v_A$. The resulting virtual short circuit at the input terminals of the op amp causes a replica of $v_A$ to appear across $R$. The circuit of Fig. 18.40 provides a relatively accurate high-input-impedance ac voltmeter using an inexpensive moving-coil meter.

### EXERCISE

**D18.34** In the circuit of Fig. 18.40, find the value of $R$ that would cause the meter to provide a full-scale reading when the input voltage is a sine wave of 5 V rms. Let meter M have a 1-mA, 50-Ω movement (i.e., its resistance is 50 Ω, and it provides full-scale deflection when the average current through it is 1 mA). What are the approximate maximum and minimum voltages at the op amp's output? Assume that the diodes have constant 0.7-V drops when conducting.

**Ans.** 4.5 kΩ; +8.55 V; −8.55 V

## 18.9.6 Precision Peak Rectifiers

Including the diode of the peak rectifier studied in Section 4.5.4 inside the negative-feedback loop of an op amp, as shown in Fig. 18.41, results in a precision peak rectifier. The diode–op-amp combination will be recognized as the superdiode of Fig. 18.35(a). Operation of the circuit in Fig. 18.41 is quite straightforward. For $v_I$ greater than the output voltage, the op amp will drive the diode on, thus closing the negative-feedback path and causing the op amp to act as a follower. The output voltage will therefore follow that of the input, with the op amp supplying the capacitor-charging current. This process continues until the input reaches its peak value. Beyond the positive peak, the op amp will see a negative voltage between its input terminals. Thus its output will go negative to the saturation level and the diode will turn off. Except for possible discharge through the load resistance, the capacitor will retain a voltage equal to the positive peak of the input. Inclusion of a load resistance is essential if the circuit is required to detect reductions in the magnitude of the positive peak.

## 18.9.7 A Buffered Precision Peak Detector

When the peak detector is required to hold the value of the peak for a long time, the capacitor should be buffered, as shown in the circuit of Fig. 18.42. Here op amp $A_2$, which should have high input impedance and low input bias current, is connected as a voltage follower. The remainder of the circuit is quite similar to the half-wave-rectifier circuit of Fig. 18.42. While diode $D_1$ is the essential diode for the peak-rectification operation, diode $D_2$ acts as a catching diode to prevent negative saturation, and the associated delays, of op amp $A_1$. During the holding state, follower $A_2$ supplies $D_2$ with a small current through $R$. The output of op amp $A_1$ will then be clamped at one diode drop below the input voltage. Now if the input $v_I$

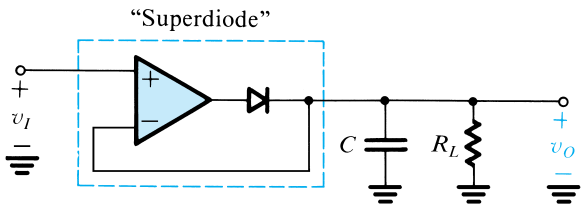


**Figure 18.41** A precision peak rectifier obtained by placing the diode in the feedback loop of an op amp.

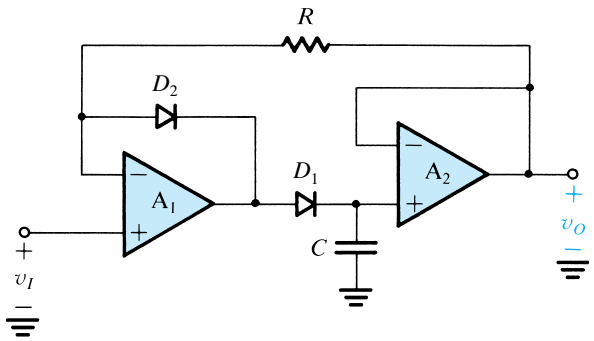


**Figure 18.42** A buffered precision peak rectifier.

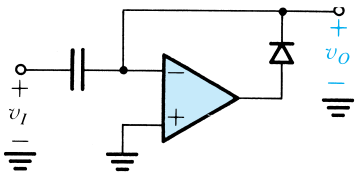


**Figure 18.43** A precision clamping circuit.

increases above the value stored on $C$, which is equal to the output voltage $v_O$, op amp $A_1$ sees a net positive input that drives its output toward the positive saturation level, turning off diode $D_2$. Diode $D_1$ is then turned on and capacitor $C$ is charged to the new positive peak of the input, after which time the circuit returns to the holding state. Finally, note that this circuit has a low-impedance output.

### 18.9.8 A Precision Clamping Circuit

By replacing the diode in the clamping circuit studied in Section 4.6.2 with a "superdiode," the precision clamp of Fig. 18.43 is obtained. Operation of this circuit should be self-explanatory.

## PROBLEMS

### Section 18.9: Precision Rectifier Circuits

**18.54** Two superdiode circuits connected to a common-load resistor and having the same input signal have their diodes reversed, one with cathode to the load, the other with anode to the load. For a sine-wave input of 10 V peak to peak, what is the output waveform? Note that each half-cycle of the load current is provided by a separate amplifier, and that while one amplifier supplies the load current, the other amplifier idles. This idea, called class B operation (see Chapter 12), is important in the implementation of power amplifiers.

**D 18.55** The superdiode circuit of Fig. 18.35(a) can be made to have gain by connecting a resistor $R_2$ in place of the short circuit between the cathode of the diode and the negative-input terminal of the op amp, and a resistor $R_1$ between the negative-input terminal and ground. Design the circuit for a gain of 2. For a 10-V peak-to-peak input sine wave, what is the average output voltage resulting?

**D 18.56** Provide a design of the inverting precision rectifier shown in Fig. 18.36(a) in which the gain is –2 for negative inputs and zero otherwise, and the input resistance is 100 kΩ. What values of $R_1$ and $R_2$ do you choose?

**D *18.57** Provide a design for a voltmeter circuit similar to the one in Fig. 18.37, which is intended to function at frequencies of 10 Hz and above. It should be calibrated for sine-wave input signals to provide an output of +10 V for an input of 1 V rms. The input resistance should be as high as possible. To extend the bandwidth of operation, keep the gain in the ac part of the circuit reasonably small. As well, the design should result in reduction of the size of the capacitor $C$ required. The largest value of resistor available is 1 MΩ.

**18.58** Plot the transfer characteristic of the circuit in Fig. P18.58.

**18.59** Plot the transfer characteristics $v_{O1}$–$v_I$ and $v_{O2}$–$v_I$ of the circuit in Fig. P18.59.

**18.60** Sketch the transfer characteristics of the circuit in Fig. P18.60.

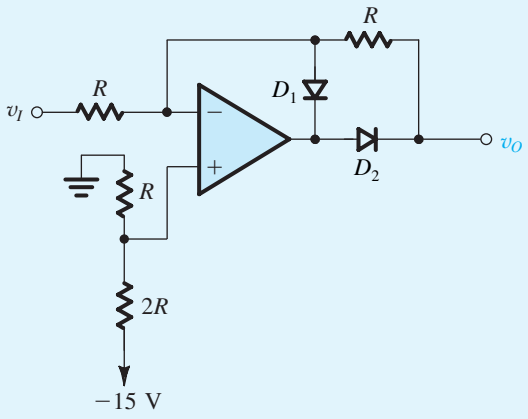


Figure P18.58

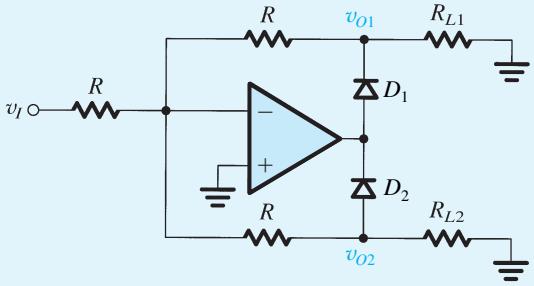


Figure P18.59

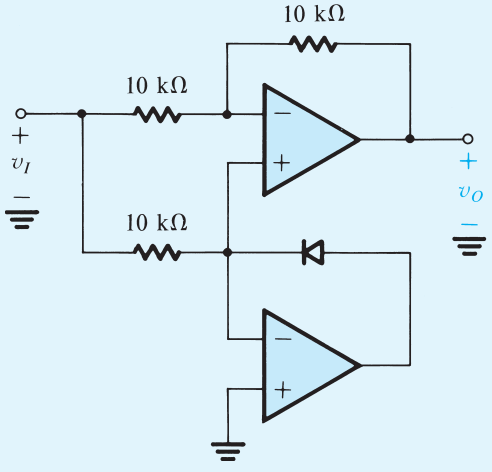


Figure P18.60

**D 18.61** A circuit related to that in Fig. 18.40 is to be used to provide a current proportional to $v_A (v_A \geq 0)$ to a light-emitting diode (LED). The value of the current is to be independent of the diode's nonlinearities and variability. Indicate how this may be done easily.

***18.62** In the precision rectifier of Fig. 18.40, the resistor $R$ is replaced by a capacitor $C$. What happens? For equivalent performance with a sine-wave input of 60-Hz frequency with $R = 1$ kΩ, what value of $C$ should be used? What is the response of the modified circuit at 120 Hz? At 180 Hz? If the amplitude of $v_A$ is kept fixed, what new function does this circuit perform? Now consider the effect of a waveform change on both circuits (the one with $R$ and the one with $C$). For a triangular-wave input of 60-Hz frequency that produces an average meter current of 1 mA in the circuit with $R$, what does the average meter current become when $R$ is replaced with the $C$ whose value was just calculated?

***18.63** A positive-peak rectifier utilizing a fast op amp and a junction diode in a superdiode configuration, and a 10-μF capacitor initially uncharged, is driven by a series of 10-V pulses of 10-μs duration. If the maximum output current that the op amp can supply is 10 mA, what is the voltage on the capacitor following one pulse? Two pulses? Ten pulses? How many pulses are required to reach 0.5 V? 1.0 V? 2.0 V?

**D 18.64** Consider the buffered precision peak rectifier shown in Fig. 18.42 when connected to a triangular input of 1-V peak-to-peak amplitude and 1000-Hz frequency. It utilizes an op amp whose bias current (directed into $A_2$) is 10 nA and diodes whose reverse leakage current is 1 nA. What is the smallest capacitor that can be used to guarantee an output ripple less than 1%?