

N-channel accumulation layer MOSFET operating at 4 K

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An accumulation layer n-channel MOSFET that operates at 4 K has been fabricated. Sharp hysteretic current kinks in the $I-V$ characteristic are observed, where the transistor switches discontinuously between two well defined states. The kinks are modelled in terms of changes in the device potential configuration due to holes generated by avalanche breakdown in the high electric field region near pinch off. Noise measurements which elucidate the physical mechanisms causing the current kinks are presented.

Keywords: low temperature electronics; transistors; hysteresis

There is a growing interest in using low temperature MOS and bipolar transistors for such applications as read out electronics for infrared detectors, fast processors and low noise amplifiers. To this end it is important to understand the physics of transport in semiconductors at cryogenic temperatures. An n-channel accumulation layer MOSFET that operates at 4 K has been fabricated. The device exhibits hysteretic two-state switching in the saturation region, which is the focus of this study.

The n-channel MOSFET differs from conventional devices in that conduction occurs through an accumulation layer that is formed at the surface of an n-type wafer, as opposed to the traditional inversion layer. Since the thermal energy is much less than the donor binding energy at LHe temperatures, the electrons in the bulk are frozen on the donor impurities. The substrate is, therefore, effectively an insulator. Application of a positive gate bias creates an accumulation layer of electrons at the oxide-semiconductor interface, forming a conducting channel from drain to source. The electrons in the channel are supplied by the degenerately doped contacts, which act as metals regardless of temperature.

The motivation for the unusual device design is to study spin dependent transport in Si. The indirect electron spin resonance experiments are discussed in Reference 1. In characterizing the transistor, hysteretic kinks in the $I-V$ characteristic, where the device switches between two well defined states, were discovered. Low temperature hysteretic kinks have been observed in conventional inversion layer n-channel MOSFETs at 4 K by Hanamura *et al.*², Dierickx *et al.*³ and Rocofyllou *et al.*⁴. The kinks in the present accumulation layer transistor differ from these observations (*Figure 2*). Most importantly, unlike the inversion devices, where there is a smooth transition from the lower to upper curve, the device switches discontinuously. In the hysteresis region, the $I-V$ characteristics of the two states do not cross in the middle, as in the inversion case^{2,3}, but remain separate. Also, the memory

effects reported in Reference 4 are not seen. For these reasons, an investigation of current kinks in our accumulation layer device was pursued to understand better the physics of transport in MOSFETs at low temperatures.

Device fabrication

The transistor was fabricated on a (100) oriented Si wafer doped with P to $3 \times 10^{17} \text{ cm}^{-3}$. A gate oxide of 74 nm was grown by dry oxidation. The source and drain contacts were implanted with As. The activated As concentration was measured to be $2 \times 10^{20} \text{ cm}^{-3}$ to a depth of $0.2 \mu\text{m}$. To obtain reproducible ohmic contacts at 4 K,

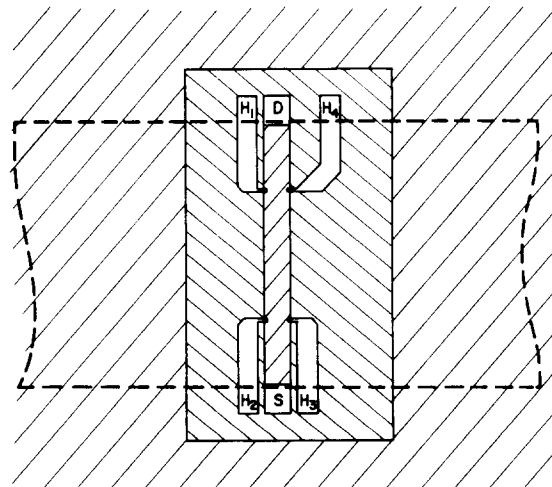


Figure 1 Top view of the MOSFET. Hall probes H_1 and H_4 are located $250 \mu\text{m}$ from the drain and probes H_2 and H_3 are $250 \mu\text{m}$ from the source

it was essential to have a high arsenic surface concentration. The gate and contact metallization consisted of a 2 μm thick sputtered Al film, followed by a 30 min anneal at 400°C in a 4% H_2 -96% N_2 atmosphere.

A top view of the FET is shown in Figure 1. The gate width is 100 μm and length is 1000 μm . The device dimensions were dictated by the requirements of the indirect electron spin resonance experiments. Four Hall probes are located along the sides of the channel to determine the electron concentration via the Hall effect. These probes can also be used to measure the potential at two points along the channel. The active area of the transistor was defined via junction isolation using a B implant of $1 \times 10^{17} \text{ cm}^{-3}$ to a depth of 0.4 μm .

I-V characteristics

Typical d.c. I-V characteristics of the MOSFET operating at 4 K are shown in Figure 2. The sweep rates are $\approx 1 \text{ V s}^{-1}$. V_G , the gate voltage with respect to the source, is 5, 6, 7 and 8 V. The substrate is left floating during the measurements. For a fixed gate bias, as the drain to source voltage V_D is increased, the transistor has a normal I-V characteristic until the drain voltage reaches a critical value V_C . At V_C , the FET switches discontinuously to a higher current, and follows the upper curve as V_D is increased further. As the drain voltage is rapidly swept back down, the transistor follows the upper curve until the two traces meet and then continues down to zero bias on the lower curve. If the transistor is biased to a point on the upper curve in the two-state region (region b in Figure 2), the device will spontaneously switch back to the lower state after a finite amount of time. The pro-

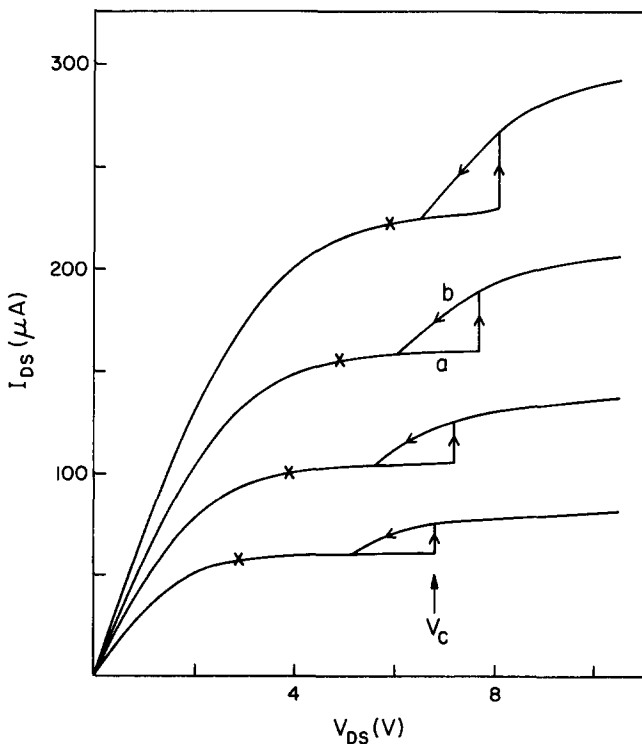


Figure 2 I-V characteristics of the MOSFET operating at 4 K, for $V_G = 5, 6, 7$ and 8 V . Threshold voltage $V_T = 2.1 \text{ V}$. x, Points where $V_D = V_G - V_T$. Labels a and b refer to the lower and upper current states in the hysteretic region, respectively

bability per unit time of switching decreases, i.e. the waiting time in the upper state increases, the closer V_D is to the critical voltage V_C . However, the device has never been observed to switch from the lower to upper state for $V_D < V_C$. The point to note here is that the FET exhibits asymmetric discontinuous switching between two well defined states.

Device physics

Avalanche breakdown

A model that explains the basic features of the hysteretic kinks can be formulated by considering the effects of the excess holes generated by avalanche breakdown in the high electric field region near pinch off. This explanation is based on a model proposed by Tihanyi and Schlotterer⁵ to explain the current kinks observed in Si on insulator (SOI) MOSFETs. The physics of our device and the SOI transistor are similar because of the presence of an insulating substrate in both cases.

Consider an FET operating in the saturation region. Define an effective gate voltage as $V'_G = V_G - V_T$, where V_T is the threshold voltage. For $V_D > V'_G$, the channel will be pinched off near the drain as shown in Figure 3. Since in saturation the device current is approximately constant, the excess drain voltage above V'_G will be dropped across the post pinch off length ΔL . As the drain voltage increases, high electric fields can build up in this region, resulting in avalanche breakdown.

Avalanche breakdown or impact ionization across the band gap can be described as follows. An electron emitted from the channel gains enough energy in the electric field before undergoing an inelastic collision to generate an electron-hole pair. The electron and hole are accelerated in opposite directions and can each lead to the formation of another electron-hole pair, resulting in carrier multiplication (Figure 4). If the electric field is high enough, a self sustaining ping-pong process can be established and catastrophic multiplication or avalanche breakdown occurs. Once an avalanche has begun, many electron-hole pairs are created and a new steady state

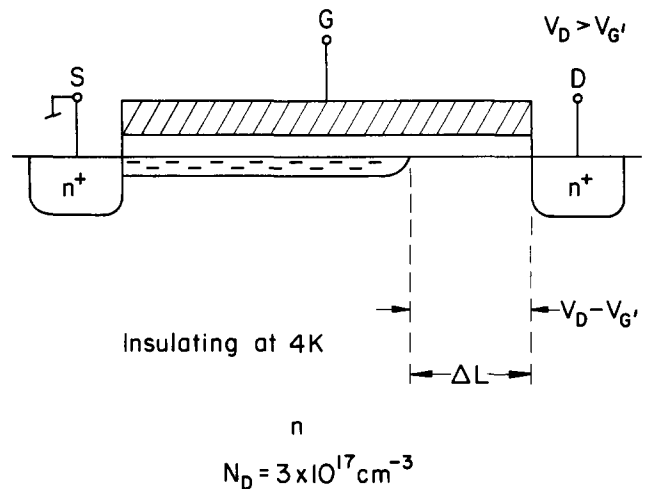


Figure 3 MOSFET potential configuration for device operating in the lower current state (a in Figure 2). $V'_G = V_G - V_T$

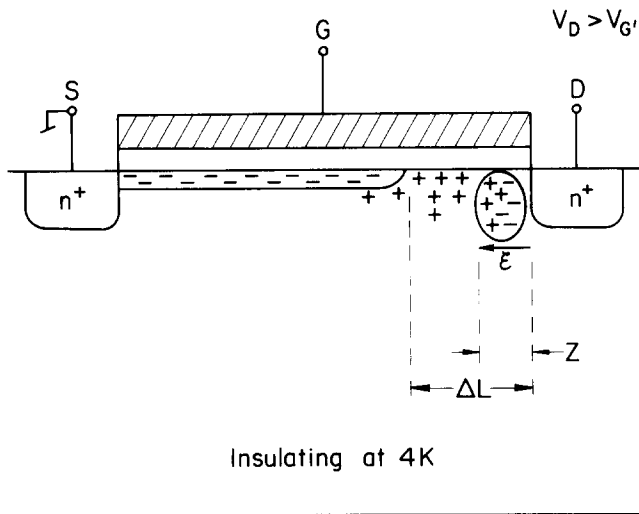


Figure 4 MOSFET potential configuration for device operating in the upper current state (b in Figure 2)

may be established in the device in which an avalanche discharge is maintained. The electrons generated in this discharge drift to the drain. The holes can drift towards the source or diffuse into the substrate. These holes, either through their own contribution to the device conductance or through their modification of the potentials defining the electron contribution to the channel conductance, result in the enhanced conductance of the device at $V > V_C$. It is important to note that for a given impurity distribution avalanche breakdown occurs at a specific value of the local electric field, giving rise to the abrupt kink in the $I-V$ characteristic. For Si the critical field⁶ is $> 3 \times 10^5$ V cm^{-1} , depending on the impurity concentration.

The data in Figure 2 are consistent with the preceding argument. For gate voltages of 5, 6, 7 and 8 V, the effective gate voltage $V'_G = 2.9, 3.9, 4.9$ and 5.9 V, respectively. Note that on all the traces the kink occurs for $V_D > V'_G$, i.e. once the channel has been pinched off near the drain. At the critical voltage V_C , avalanche breakdown occurs and the device switches to a new characteristic.

Measurements from several devices suggest that the value of V_C depends on the specific impurity configuration of the channel near the drain electrode. Comparison of the $I-V$ characteristics, below V_C , of several devices shows them to be identical within the precision of the measurements. On the other hand, the critical voltages are found to vary by as much as 1 V from device to device, suggesting that the statistical fluctuations of impurities or dopants in a small breakdown region, rather than average properties, are important in defining the breakdown condition. The resultant excess current flow is filamentary in nature. The arguments are the same as those used in discussion of the microplasmas⁷ observed at breakdown in reverse biased Si junctions.

Figure 5 illustrates a result supporting the filamentary current model. The continuous line shows the $I-V$ characteristic for device 1 at $V_G = 6.0$ V. The dotted line shows the characteristic for a different device (2) at the same gate bias. Although the characteristics below breakdown are identical, in the hysteresis region a different curve is obtained. In particular, two kinks are observed, suggesting that breakdown occurs at two points across the

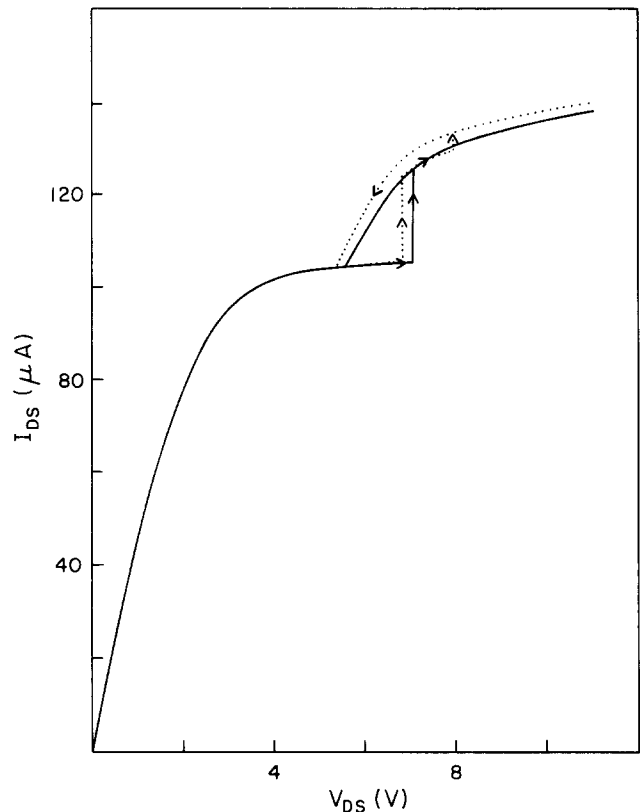


Figure 5 $I-V$ characteristic for device 1 (—) and device 2 (····)

drain contact. These data indicate that the breakdown voltage is a function of the impurity distribution of the particular device.

Excess hole distribution

Avalanche breakdown effects have been shown to switch the transistor from the lower state to the upper state at V_C . What physical mechanisms are responsible for the device behaviour above V_C and also below V_C in the hysteretic region? An answer can be found by considering the holes generated by avalanche breakdown.

For $V_D > V_C$ electron-hole pairs are generated in a high field region adjacent to the drain as shown in Figure 4. The electrons are swept into the drain contact. Since the drain potential is higher than the gate potential, there exist electric field lines in the space charge region that originate at the drain and terminate at the gate along the length ΔL . Mobile holes generated by avalanche are swept into all, or at least a portion of, the pinch-off region ΔL , converting it into a conducting channel. The resultant reduction in the voltage drop across ΔL forces a larger current through the device to maintain the total source-drain voltage drop equal to the applied voltage.

An alternative possibility is the drift and/or diffusion of holes into the substrate below the source channel. Build up of positive charge in the substrate raises the substrate potential, which is equivalent to reducing the threshold voltage. Such a threshold shift, even without the effects of holes near the drain, would result in an increased device current. Measurements of the device potential along the channel, using the Hall probes located at a distance $0.25L$ and $0.75L$ from the source (see Figure 1), were made to discriminate between these two mechanisms. Within the

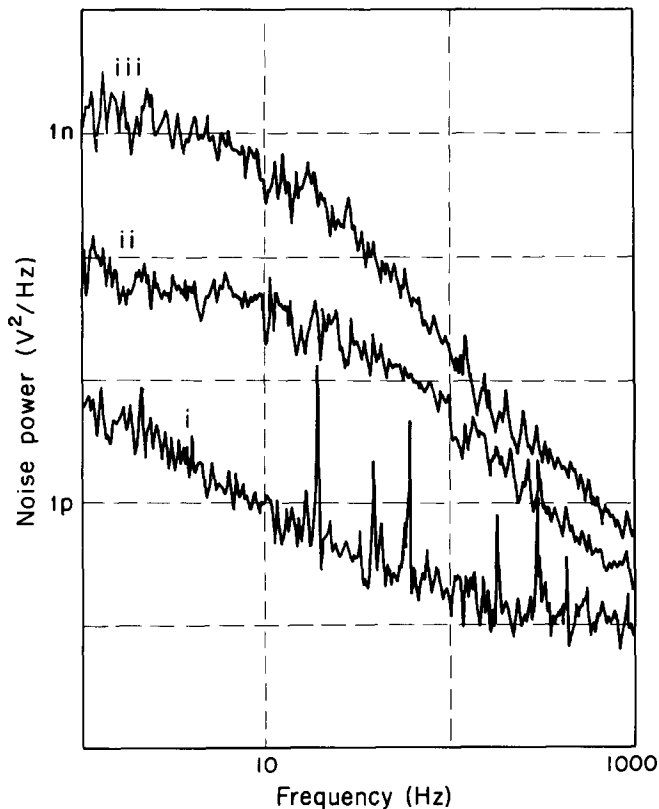


Figure 6 Noise power as a function of frequency for $V_G = 6.0$ V. Transistor is operating in the lower current state for trace (i) and in the upper current state for traces (ii) and (iii). $V_D = 6.9$ V, 7.0 V and 6.3 V for traces (i), (ii) and (iii), respectively

framework of the gradual channel approximation, the increase in current at the kink and the measured probe voltages can be modelled as a decrease in the effective channel length without changing the threshold voltage. This indicates that over the first three quarters of the device the current kink is due primarily to the contribution of holes adjacent to the drain as opposed to trapped holes in the source region.

Can the creation of the conductivity modulated region account for the observed behaviour of the transistor in the hysteretic region? As V_D is swept down, the FET remains on the upper curve (labelled b) in *Figure 2* for a finite amount of time. The FET acts as if once avalanche breakdown occurs the avalanche process can be sustained at a lower drain bias than that necessary for the initial breakdown. *Figure 4* shows that as V_D is lowered below V_C the conductivity modulated region, which acts as a short circuit in series with the channel, still persists. Suppose the situations before (*Figure 3*) and after (*Figure 4*) the kink are compared at the same drain bias. After the kink the excess voltage $V_D - V_G'$ is dropped across the shorter region of length z as opposed to the longer region ΔL before the kink. Therefore, in the upper current state, electric fields large enough to cause avalanche breakdown can be maintained at V_D values below V_C required to initiate breakdown. However, in the lower current state they cannot.

The transistor has been observed to switch from curve b in *Figure 2* to curve a, but has never been seen to switch up. This occurs because the upper state is metastable with respect to large fluctuations in the avalanche region. A

fluctuation in the breakdown region results in reduced hole injection into the conductivity modulated region. A larger fraction of $V_D - V_G'$ is dropped across the conductivity modulated region, so the electric field in the avalanche region decreases further. For large enough fluctuations the positive feedback can quench the avalanche breakdown and the transistor switches from the upper to the lower state. The instability of the upper state in the hysteretic region is substantiated by noise measurements.

Noise measurements

In *Figure 6* the measured noise power as a function of frequency is shown for a gate bias of 6 V. For the device biased into saturation but before the kink, the low frequency noise in curve (i) has an approximately $1/f$ type of spectrum, which is typical for Si MOSFETs⁸. In the upper current states the low frequency noise power, curves (ii) and (iii), increases by a factor of $10-100$. Comparison of curves (ii) and (iii) demonstrates the increasing instability of this state as the drain bias moves downwards away from V_C . This type of noise spectrum, which is constant at low frequencies and falls off with an RC-type roll-off is typical of generation recombination (GR) noise⁸. One possible postulate is that traps in the substrate that have captured the avalanche generated holes are responsible for the GR like noise spectrum.

Conclusions

Measurements of an accumulation layer n-channel MOSFET operating at 4 K have been presented. The observed current kinks were modelled in terms of changes in the device potential configuration caused by the excess holes generated from avalanche breakdown at the drain. After breakdown, the device current flow appears to be filamentary in nature. Within the gradual channel approximation the noise and potential measurements indicate that the increased current in the upper state is due primarily to the development of a highly conducting region near the drain, which forces a decrease in the channel length. Threshold shifts due to hole accumulation along the first three quarters of the device are of secondary importance.

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