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High Frequency Inversion Capacitance Measurements for 6H-SiC n-MOS Capacitors from 450 to 600 °C

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Abstract

The operation of metal-oxide-semiconductor (MOS) devices based on the semiconductor SiC in high temperature environments above 300 °C requires an understanding of the physical processes in these capacitor structures under operating conditions. In this study we have focused on the regime of inversion biasing, where the electrical characteristics of the device are dominated by minority carriers. We report on the direct observation of the high frequency inversion capacitance due to thermal generation of holes in 6H-SiC n-MOS capacitors between 450 and 600 °C by monitoring the 1MHz C-V characteristics of large area, 1000 μm diameter, capacitors in the dark. Our experimental results are consistent with a first order calculation based on the delta depletion approximation.

Introduction

SiC based field-effect structures show great promise for electronic and sensing applications at elevated temperatures. Device design requires an understanding of the physical processes in these capacitor structures at the operating temperature. In this study we have focused on the regime of inversion biasing, where the electrical characteristics of the capacitor are dominated by minority carriers. Due to the large bandgap of SiC (3.00 eV for 6H-SiC), minority carrier generation/recombination rates are rather sluggish, which in turn means that the time constant for the semiconductor to reach equilibrium can be quite long. The physics of inversion layers in 6H-SiC has been studied up to ~400 °C using high frequency capacitance-voltage (C-V) techniques, transient capacitance measurements and the Hall effect [1,2,3,4,5]. In 4H-SiC inversion capacitance in both n-MOS and p-MOS devices have been observed via capacitance-transient techniques [6].

We report on the direct observation of the high frequency inversion capacitance due to thermal generation of holes in 6H-SiC n-MOS capacitors between 450 and 600 °C. In order to ensure that the minority carriers were thermally generated we measured the 1MHz C-V characteristics of large area, 1000 μm diameter, capacitors in the complete absence of light.

Experimental

The n-MOS capacitors were fabricated on 1cm^2 6H-SiC (0001) Si face substrates with a 5.1 μm, 9.44 x 10^{15} N/cm^3 epitaxial layer grown on an n+ wafer. The gate oxide was grown by dry oxidation at 1150 ºC for 6 hours at 1 atm in a 500 sccm dry O_2 gas stream. This was immediately followed by a 30 min 1150 ºC Ar anneal and a 2 hour 1175ºC post oxidation NO passivation anneal in pure NO (577 sccm) at 1 atm. The oxide thickness as determined by spectroscopic ellipsometry is 46.1 nm. The gate metal is 100 nm of Pt sputtered at 350 ºC in a 2.5 mTorr Ar atmosphere.

The SiC chip has an array of 52 gates with nominal diameters ranging from 200 to 1000 μm, all the data in this report are from a single 1065 ± 5 μm device. A large area back contact provides a common ground plane.

The SiC sample was mounted on a thermally conducting alumina header with three backside platinum microheaters (Heraeus) to locally heat the 1cm^2 SiC sample to 630 ºC. The temperature of the Pt gate was determined by monitoring the resistance of the backside heater. We estimate that our uncertainty is +5/-10 °C after accounting for the measured thermal impedance between heater and Pt gate. The alumina header provided the necessary electrical insulation from the heater current for precision 1MHz C-V measurements (Keithley Model 590). At 630 ºC our noise is ±2pF. All measurements were made in the dark, inside a light tight enclosure.

Results and Discussion

Shown in Fig. 1 are the high frequency (1MHz) C-V characteristics of a 1065 μm diameter n-type capacitor in the *dark*, at various temperatures between 300 – 600 °C, normalized with respect to the oxide capacitance C_{ox}. Following a 10 s hold in accumulation, the curves were swept from positive to negative bias at 0.40 V/s. At all temperatures we obtain a well defined C-V characteristic in accumulation. Note that the measurements were made without using optical illumination to generate minority carriers.

From standard MOS capacitor analysis there are two limiting cases we expect to encounter as the device is ramped from depletion to inversion bias, where a large number of minority carriers (holes) are needed to establish an equilibrium charge distribution within the MOS capacitor. As the measurements are performed in the dark, any minority carriers must be created by generation processes within the SiC epi-layer near the SiC/oxide interface. Case 1: if the temperature is high enough and the ramp rate is slow enough, the semiconductor will reach equilibrium due to thermally generated minority carriers and an inversion capacitance that is the sum of the oxide and semiconductor capacitances will be measured. Case 2: if the temperature is too low for thermal generation of minority carriers the semiconductor will be driven into non-equilibrium or deep depletion conditions. At 603, 550 and 453 °C the capacitance under inversion bias is a constant independent of voltage for $V_{gate} < -1.1$ V as shown in Table 1. At 305 °C the semiconductor is driven into deep depletion. For the 400 °C curve the MOS capacitor is in some intermediate state under inversion bias, based on $1/C^2$ analysis to be presented in the next section.

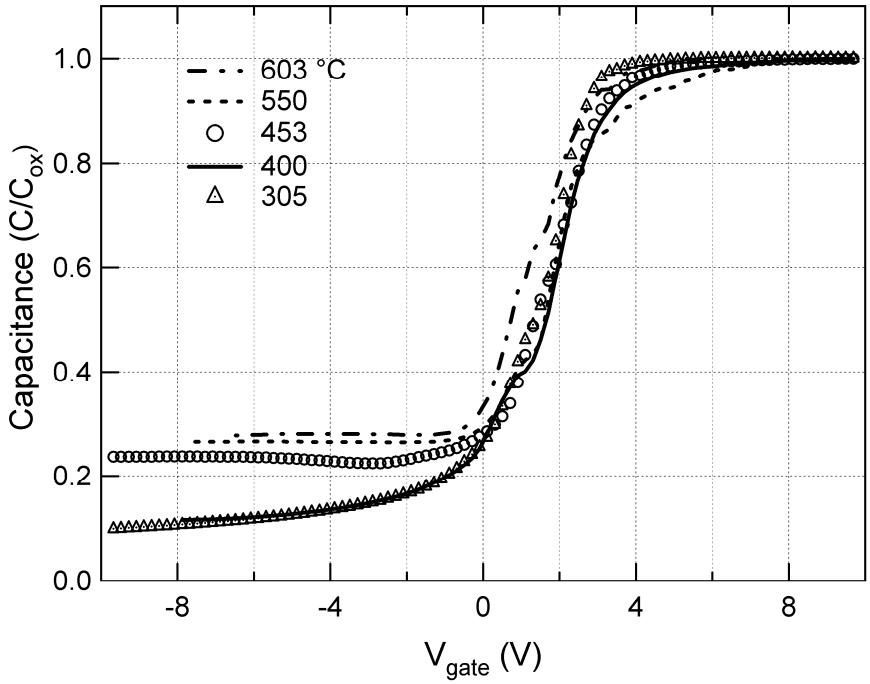

Fig. 1, 1MHz C-V curves of a 1065 μm diameter 6H-SiC n-MOS capacitor from 305 to 603 °C. Measurements were made in the dark from positive to negative bias at a sweep rate of 0.40 V/s.

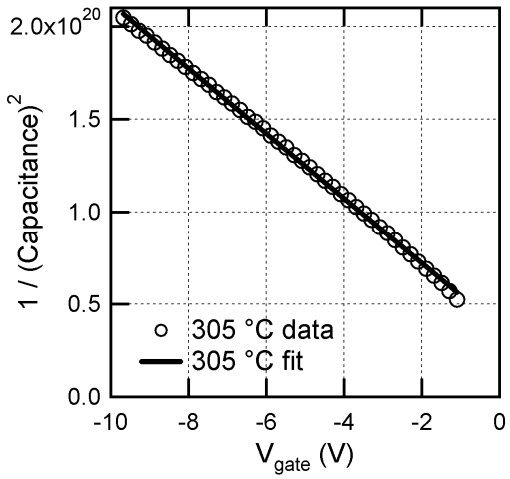

Fig. 2, $1/C^2$ analysis at 305 °C, a least squares fit gives a slope that agrees with the nominal doping density reported by the crystal grower.

The effective majority carrier density in the SiC epi-layer was determined to be (10.2 ±0.5) x $10^{15}/cm^3$ at 305 °C via $1/C^2$ analysis [7], from Fig. 2. This is consistent with the donor doping density of 9.44 x 10^{15} N/cm^3 reported by the crystal grower. Note that at 400 °C, $1/C^2$ analysis does not yield a good linear fit in inversion, leading us to speculate that at this temperature the device is in some intermediate state between Case 1 and Case 2.

The inversion capacitance at high temperature was calculated using the delta depletion approximation, which assumes that the free carrier distribution in the transition region between the depletion region and the neutral bulk can be approximated by a step function [7]. In addition we assumed that the minority carrier (hole) density at high temperature (>453 °C) is independent of temperature and can be approximated by the measured effective majority (electron) carrier concentration at 305 °C. The resultant inversion capacitances, normalized with respect to C_{ox}, are given in Table 1. Also in Table 1 are the experimental values obtained from the inversion region of the measured C-V curves, $V_g < -1.1V$ in Fig. 1; again normalized with respect to C_{ox}. As expected from theory the measured inversion capacitance decreases with temperature from 603 to 453 °C. The experimental numbers agree with the calculated values within the level of approximation of our model. We speculate that at the higher temperatures of 603 and 550 °C, the measured capacitance is larger than that predicted by our model because the number of minority carriers in the semiconductor is actually larger than the number of majority carriers measured at 305 °C, due to the negative temperature dependence of the bandgap.

Table 1: High temperature inversion capacitance

Temperature (°C)	$C_{inversion}/C_{ox}$ (experiment)	$C_{inversion}/C_{ox}$ (model)
603	0.279 ± 0.002 [-6.5 < V_g (V)< -1.1]	0.241
550	0.266 ± 0.002 [-7.5 < V_g (V)< -1.1]	0.232
453	0.235 ± 0.010 [-9.7 <V_g (V)< -1.1]	0.219

High temperature inversion capacitance: (i) experimental data from Fig. 1 with the range of gate bias and (ii) results from model.

Conclusions

We have experimentally observed the high frequency inversion capacitance, due to thermal generation of minority carriers, in an n-MOS 6H-SiC capacitor between 600 and 453 °C. The data was obtained from C-V measurements performed in the dark. At high temperature, > 453 °C, the measured inversion capacitance increases with increasing temperature. This is consistent with a first order calculation using the delta depletion approximation.

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